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MS-7681

ATX(Full Size)
Ver: 0A

CPU:
INTEL - Sandy Bridge LGA 1155

System Chipset:
INTEL - Cougar Point PCH

OnBoard Chipset:
Clock Gen:IDT 4106
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000 NIC X 2
SIO:FIN71889AD
ESATA Controller: JM363
USB3.0: UPD720200F1
Flash ROM: 64 Mb SPI (PCH)
1394 Controller: VT6308P

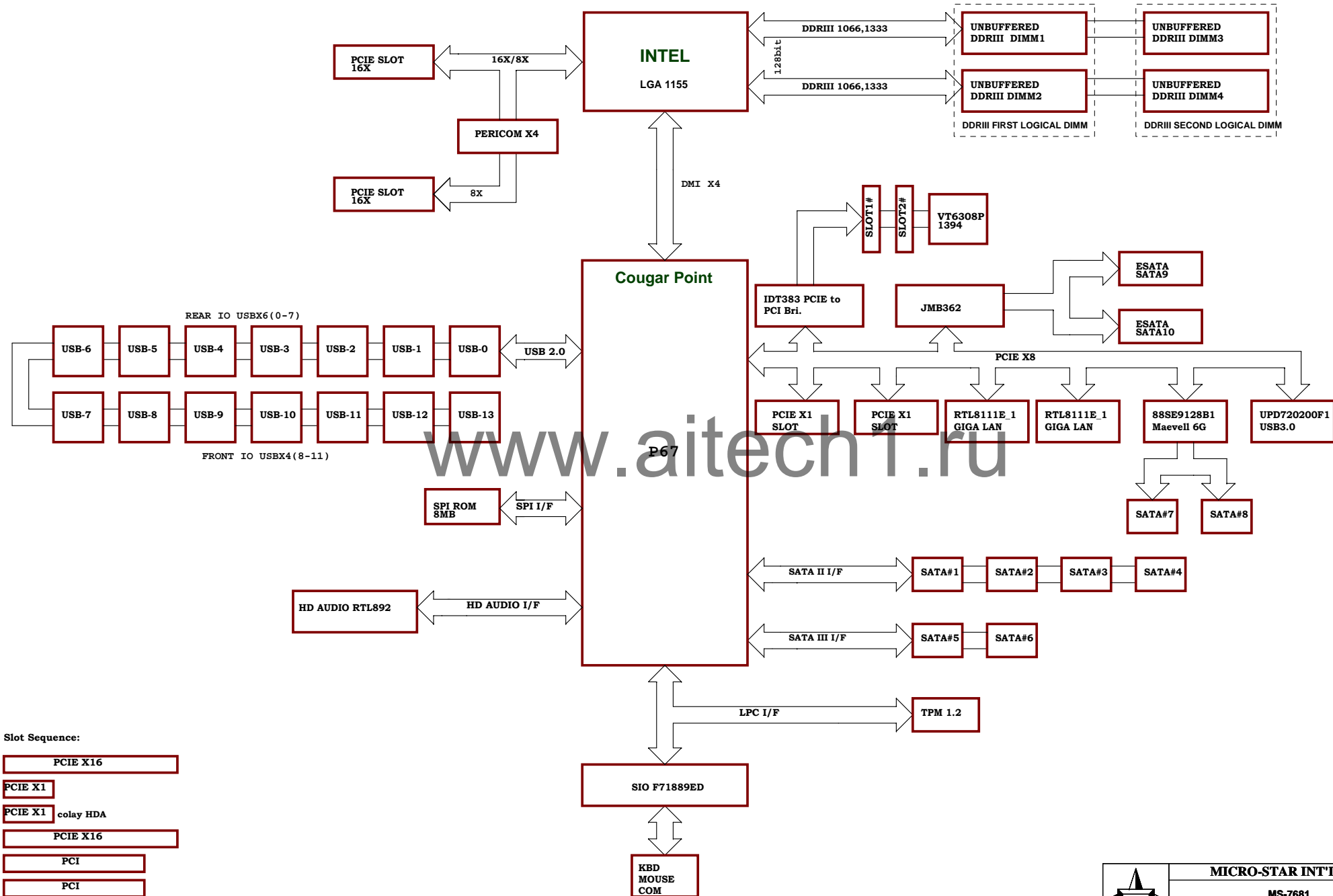
Main Memory:
DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:
PCI Express (X16) Slot * 2
PCI Express (X1) Slot * 3
PCI Slot * 2(From IDT TSI383)

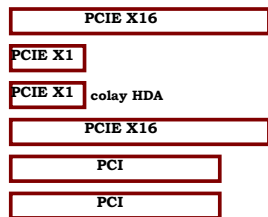
PWM:
CPU:UPI6234(5PHASE)
CPU_VTT:UP6113A(1PHASE)
CPU_SA:UP6113A (1PHASE)
DDR/PCH PWR:UP6103A

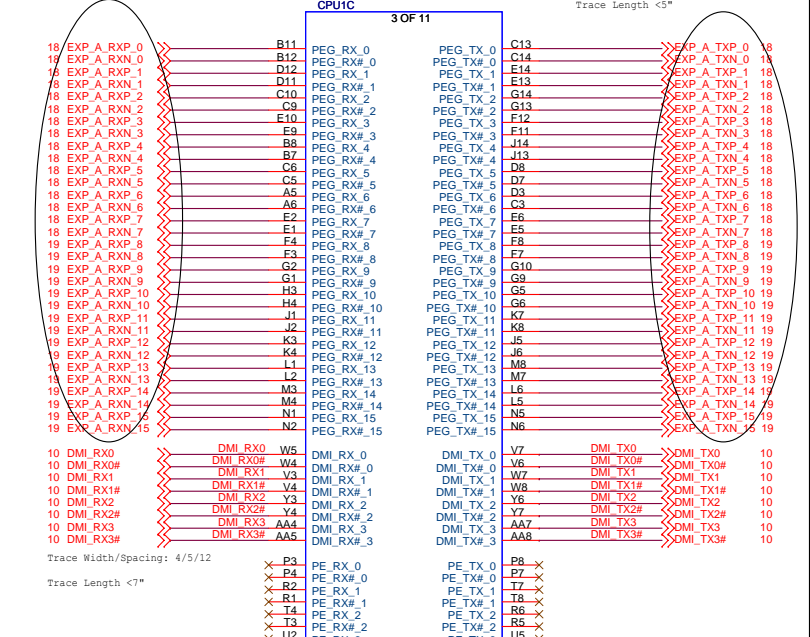
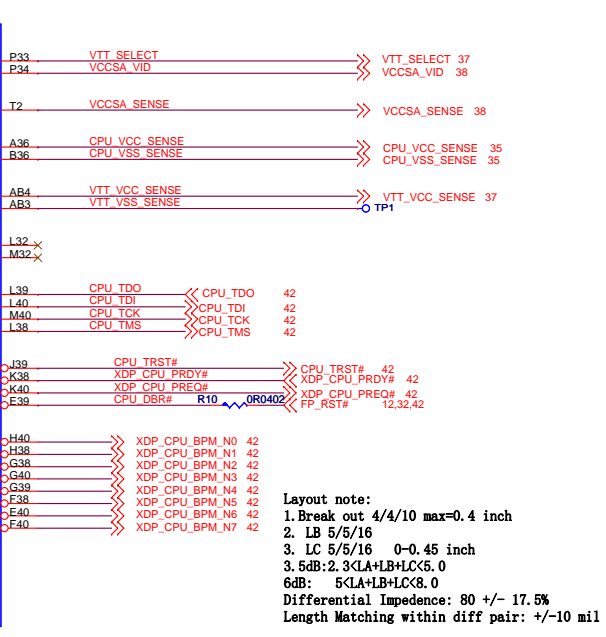
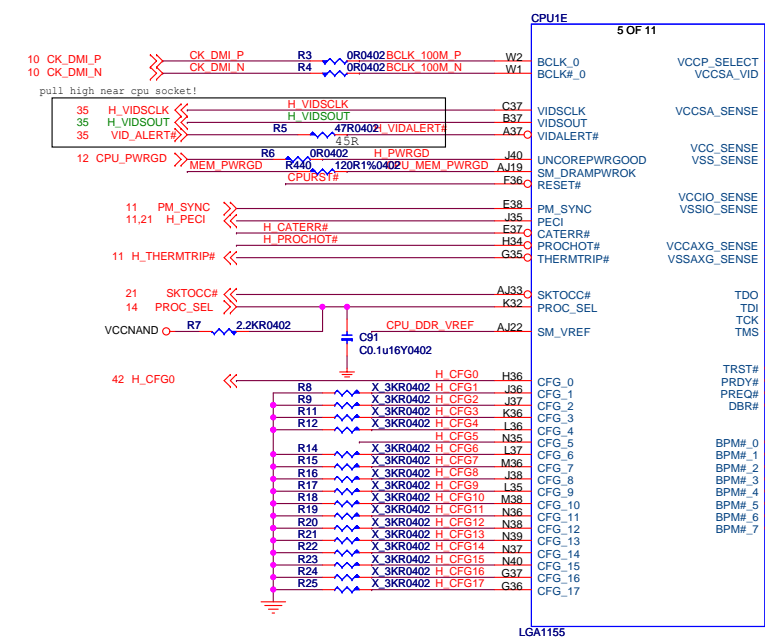
ACPI:
UPI

Other:
SATA3.0 x2+SATA2.0 x4 (PCH)
ESATA2.0 x2 (JMB363)
USB2.0 *4 (Rear*8 Front*4)
COM Header *1
USB3.0 *4 (Rear*2 Front*2)

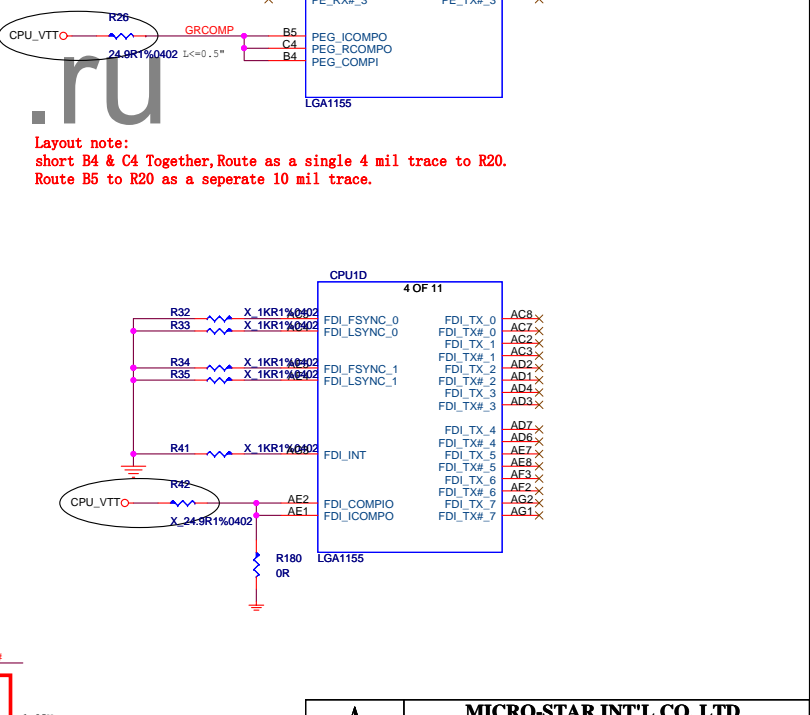
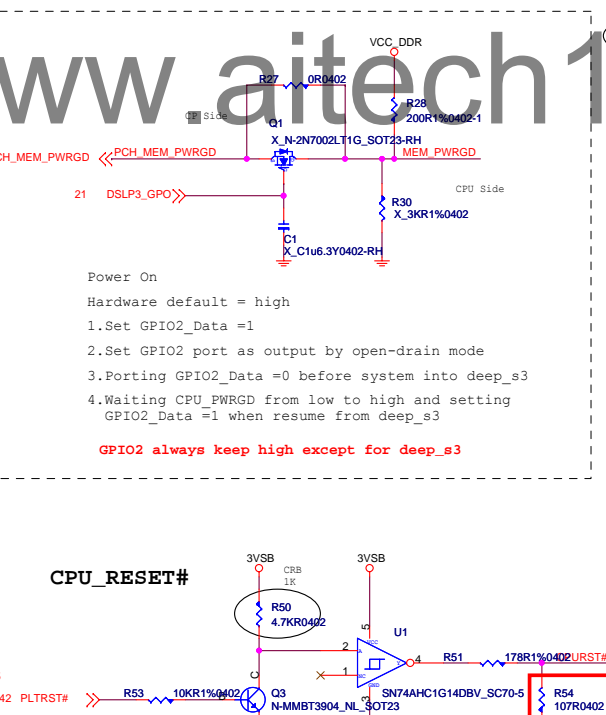
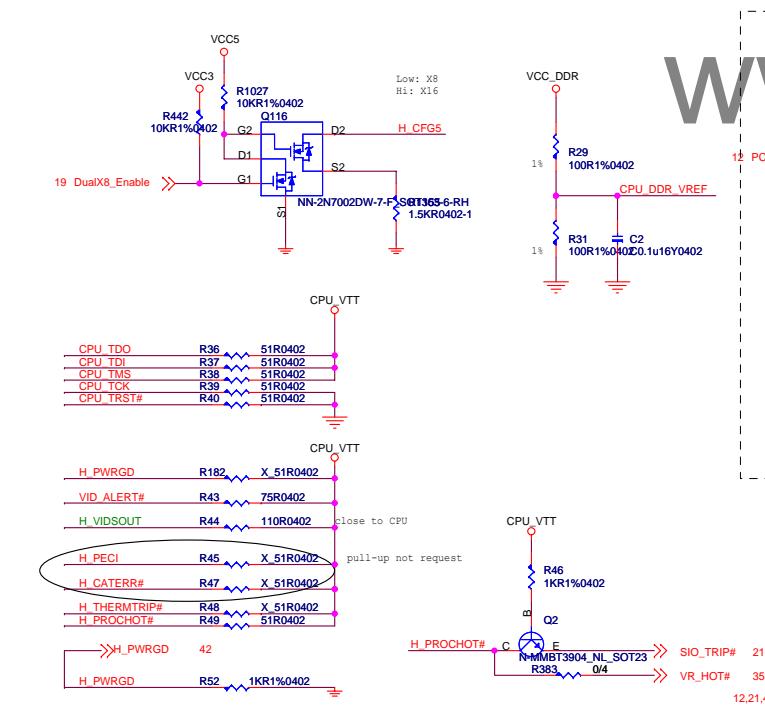


Slot Sequence:

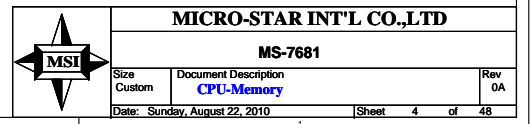


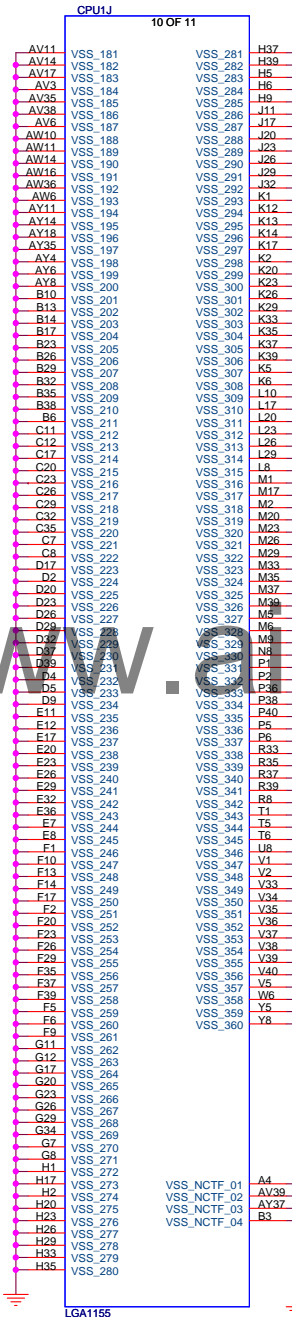
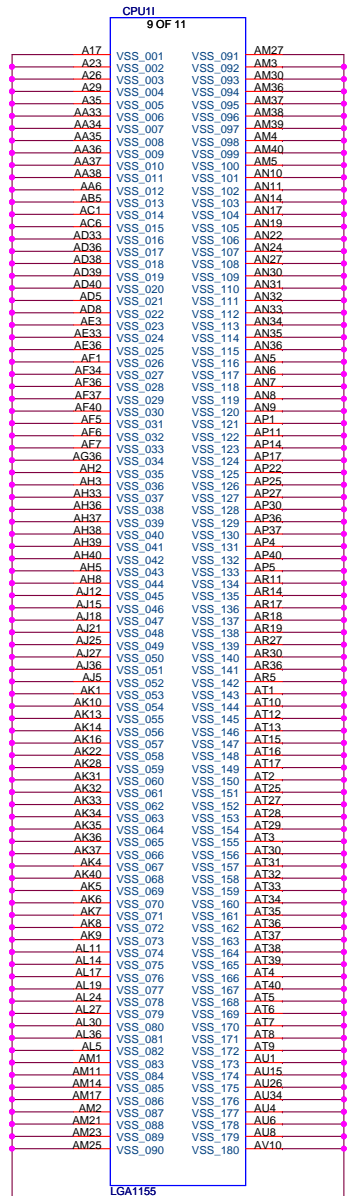


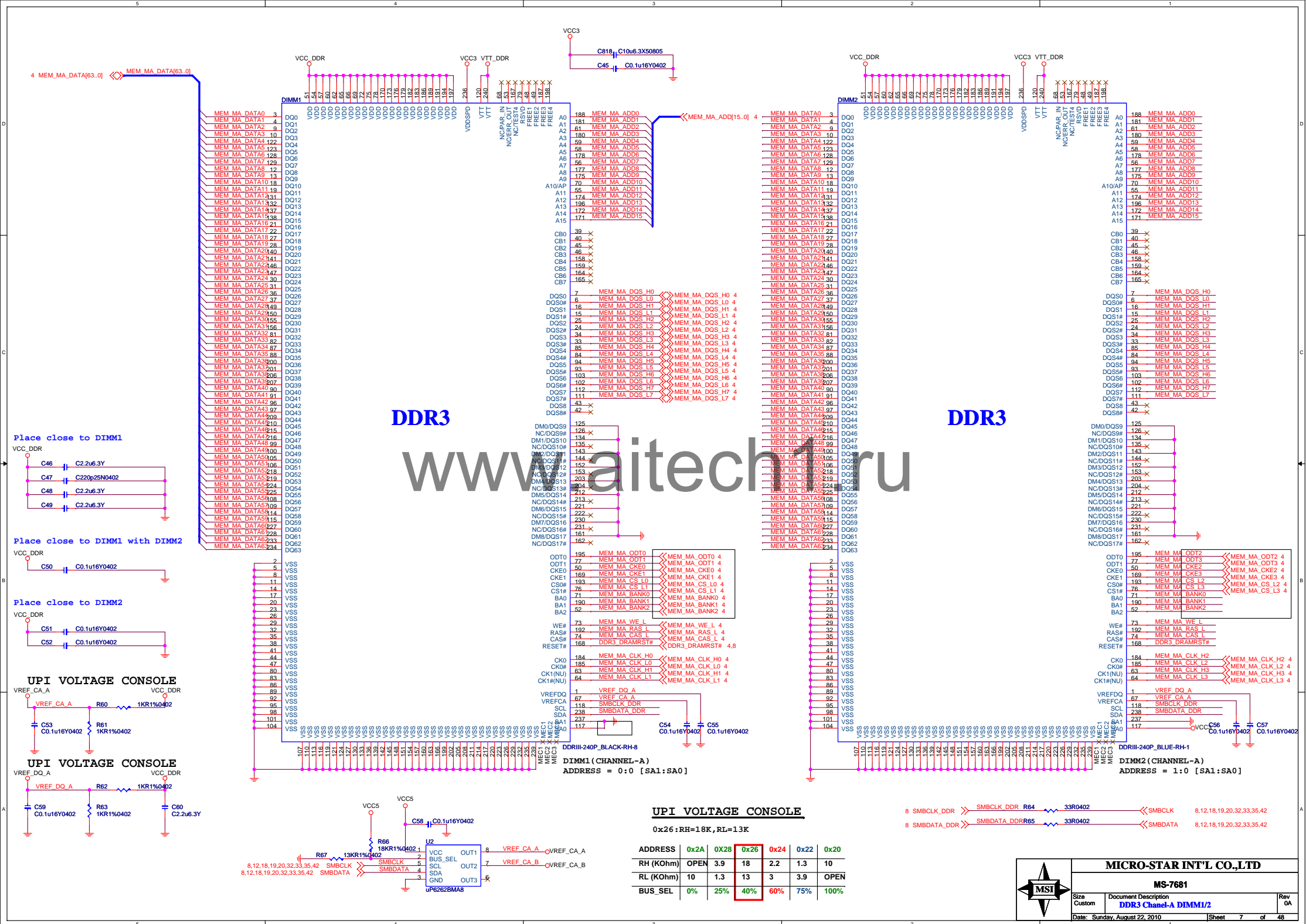
Layout note:
1. Break out 4/4/10 max=0.4 inch
2. LB 5/5/16
3. LC 5/5/16 0-0.45 inch
3. 5dB: 2.3<LA+LB+LC<5.0
6dB: 5<LA+LB+LC<8.0
Differential Impedance: 80 +/- 17.5%
Length Matching within diff pair: +/-10 mil



PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

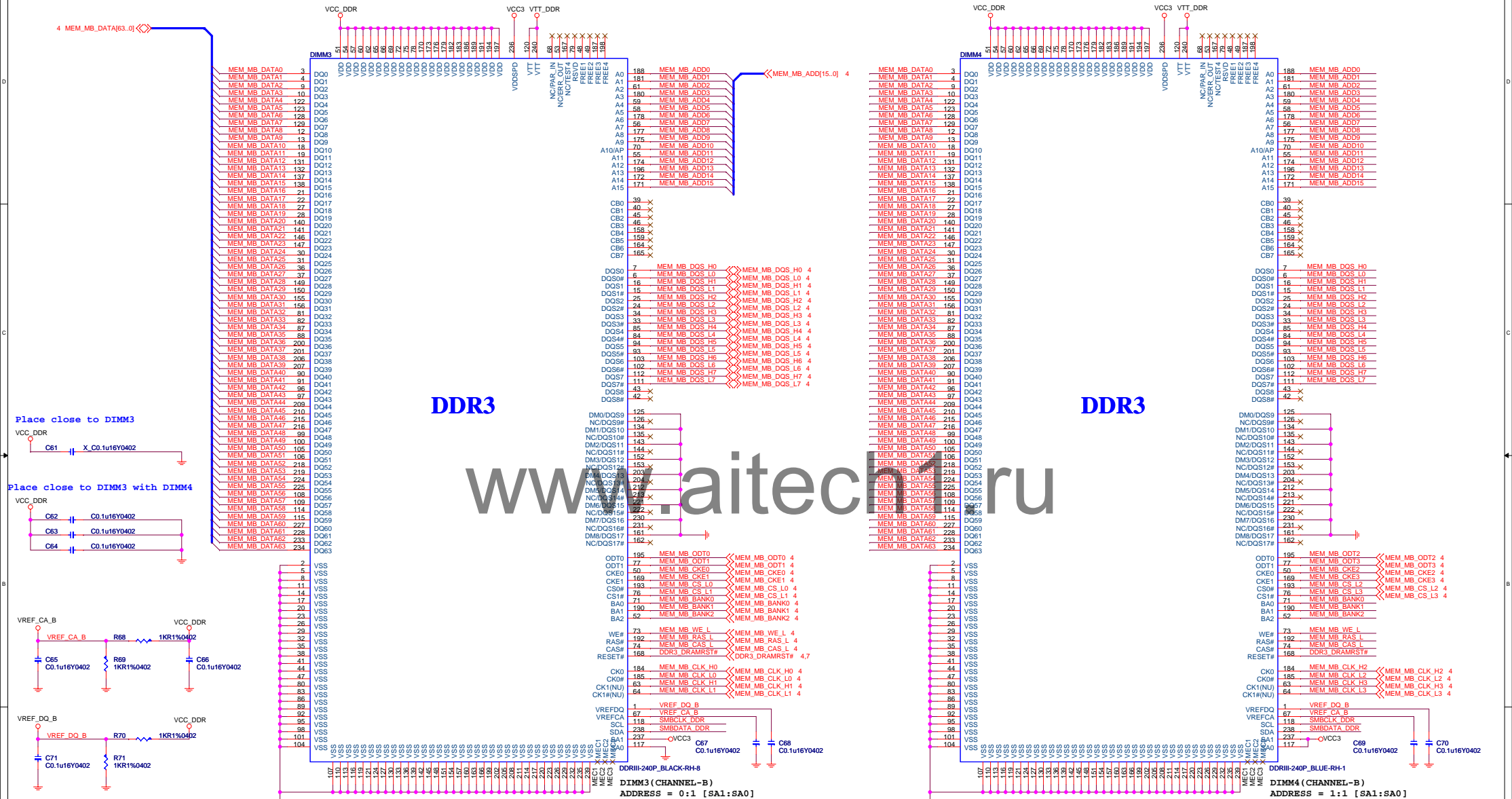






DDRIII DIMM_B0

DDRIII DIMM_B1



UPI VOLTAGE CONSOLE


0x28:RH=9.1K,RL=3K

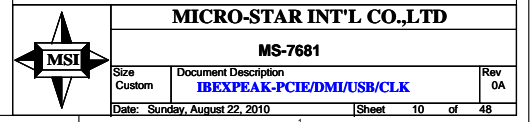
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

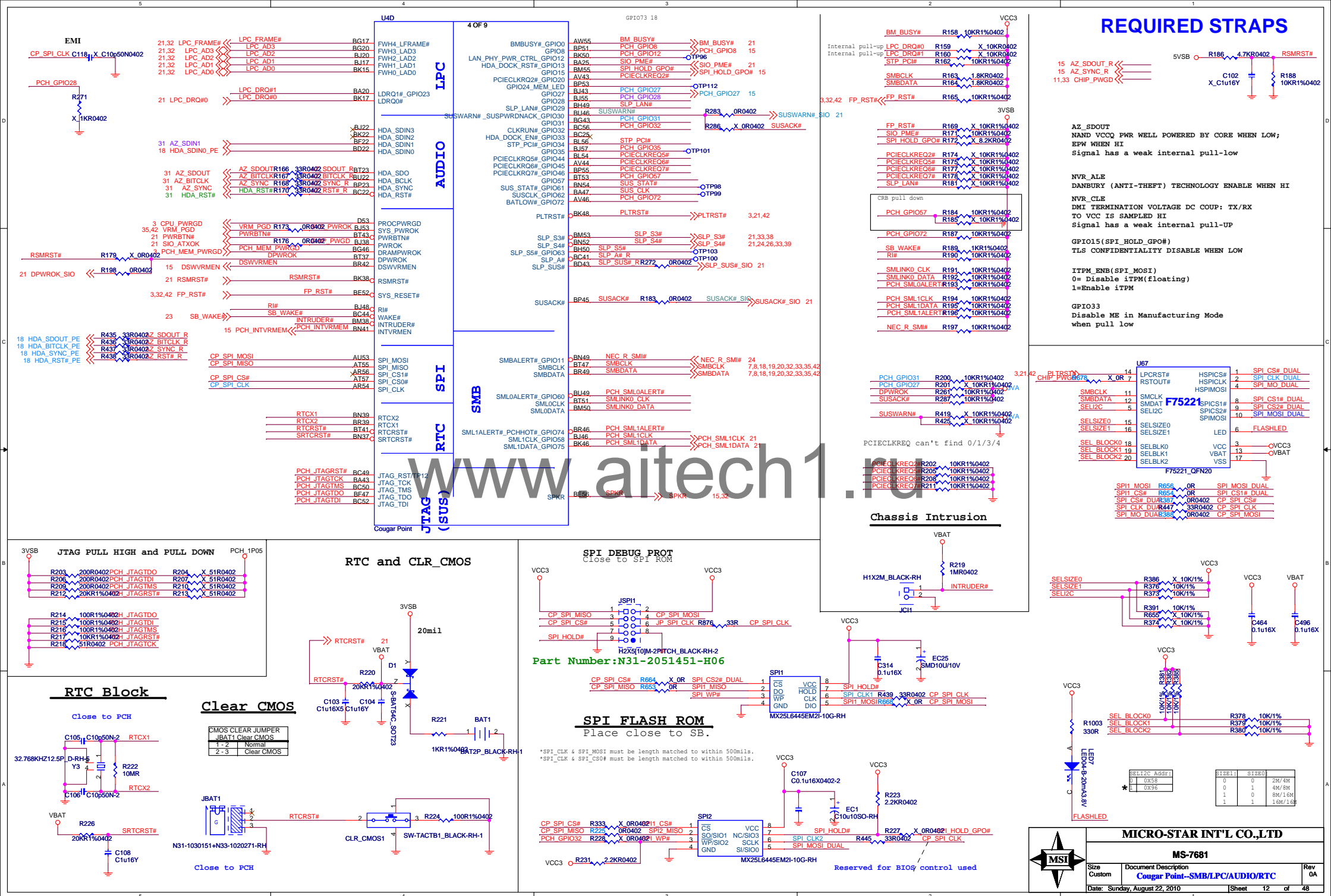


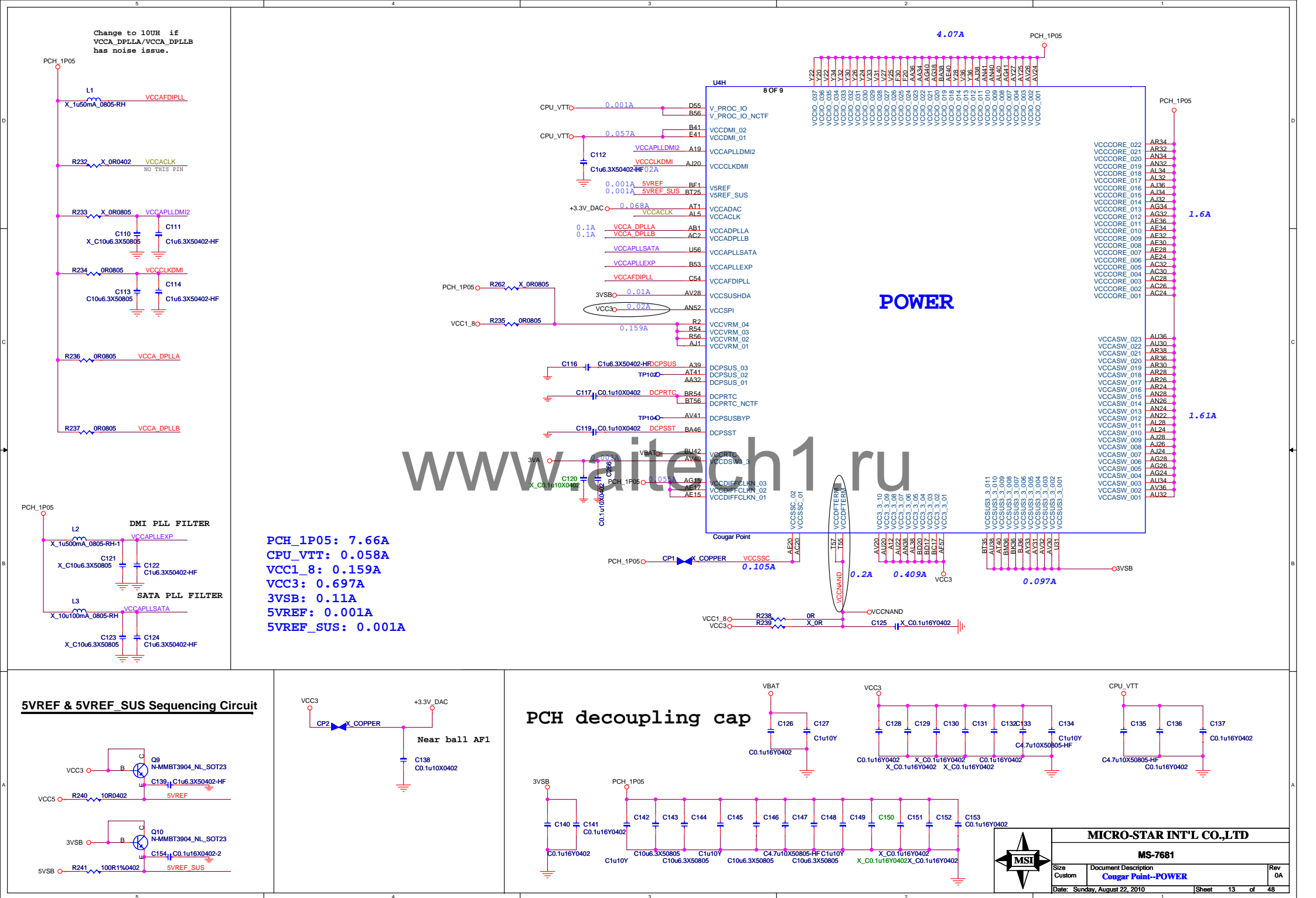
MICRO-STAR INT'L CO.,LTD		
MS-7681		
Size	Document Description	Rev
Custom	DDR3 Chnel-B DIMM3/4	0A
Date:	Sunday, August 22, 2010	Sheet 8 of 48

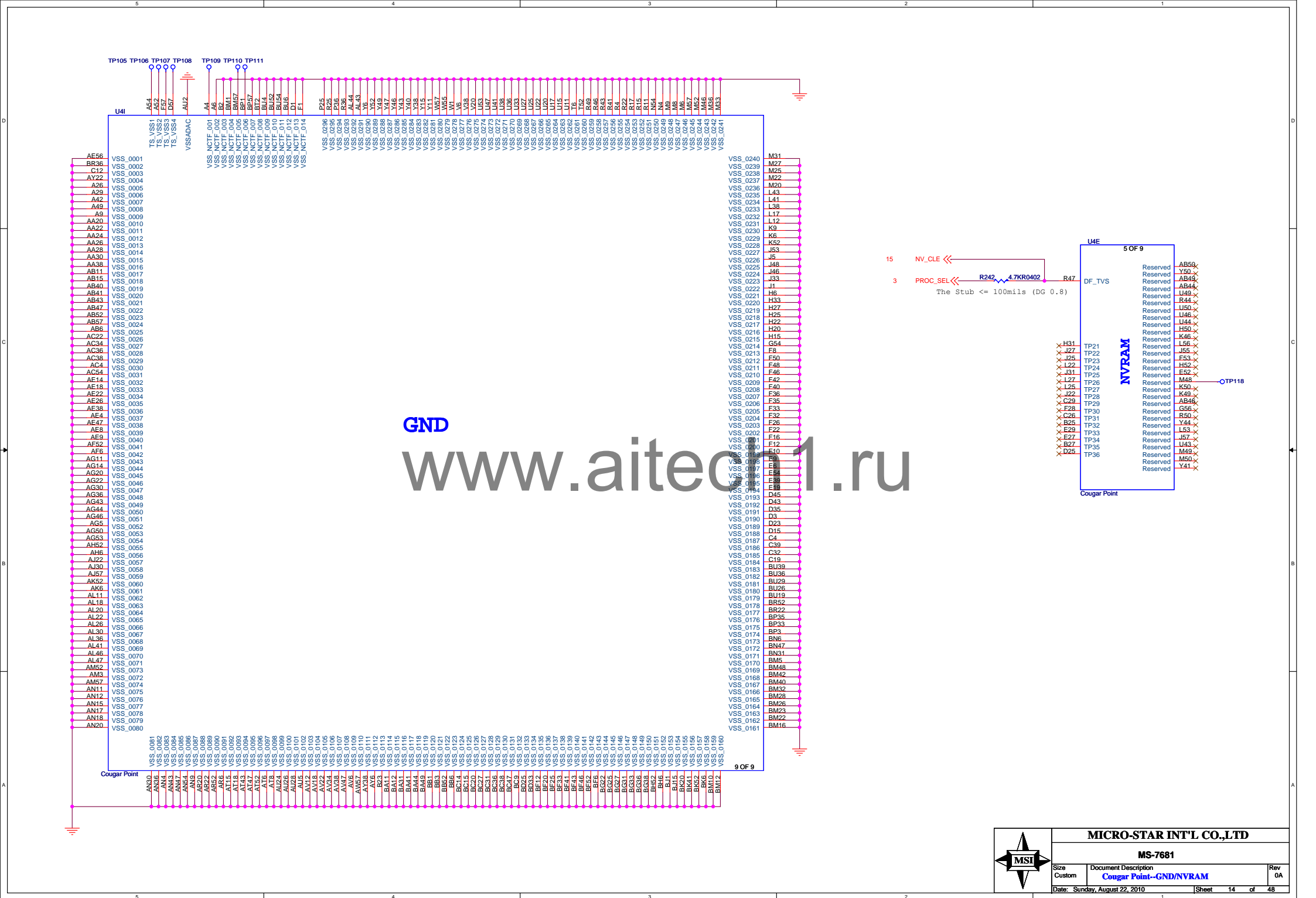
www.aitech1.ru

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			MS-7681	
Size	Document Description			Rev
Custom	CLK ICS9LR54105B			0A
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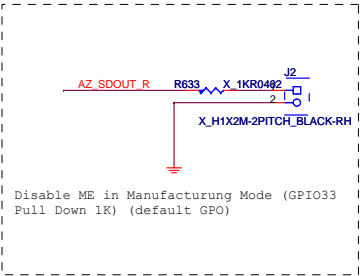
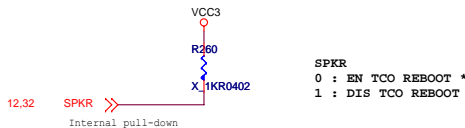
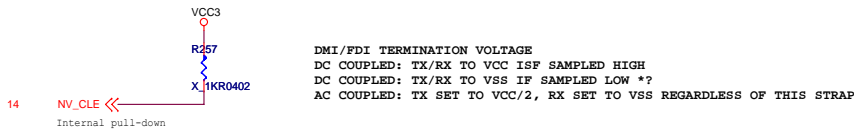
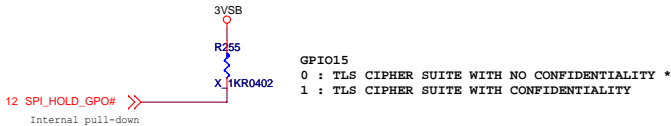
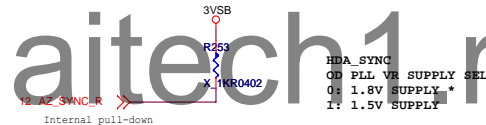
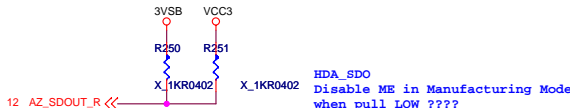
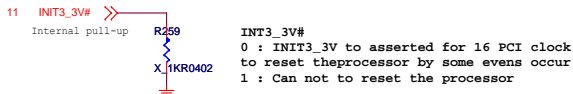
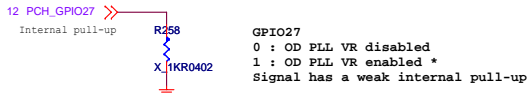
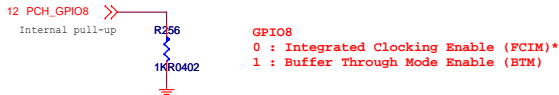
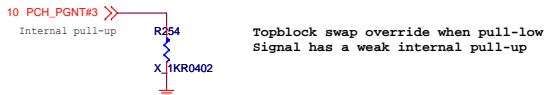
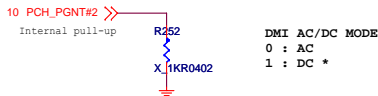
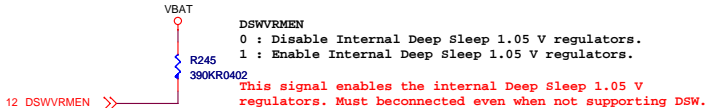
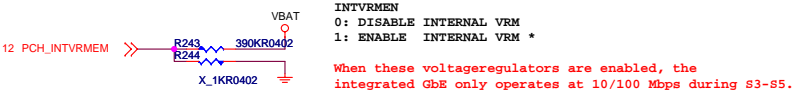
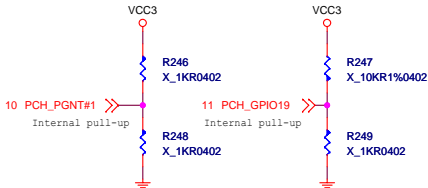




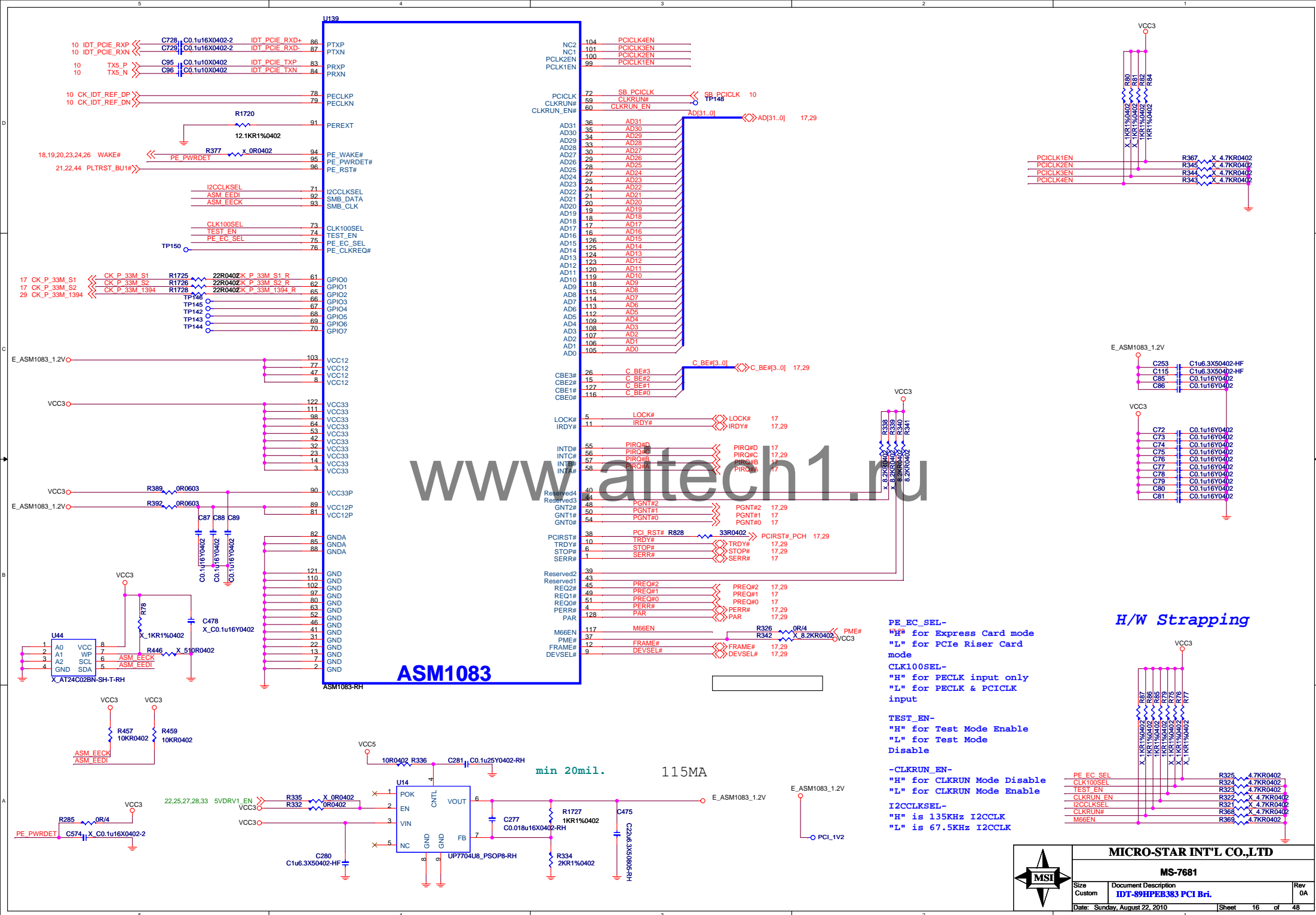


PCH Straps

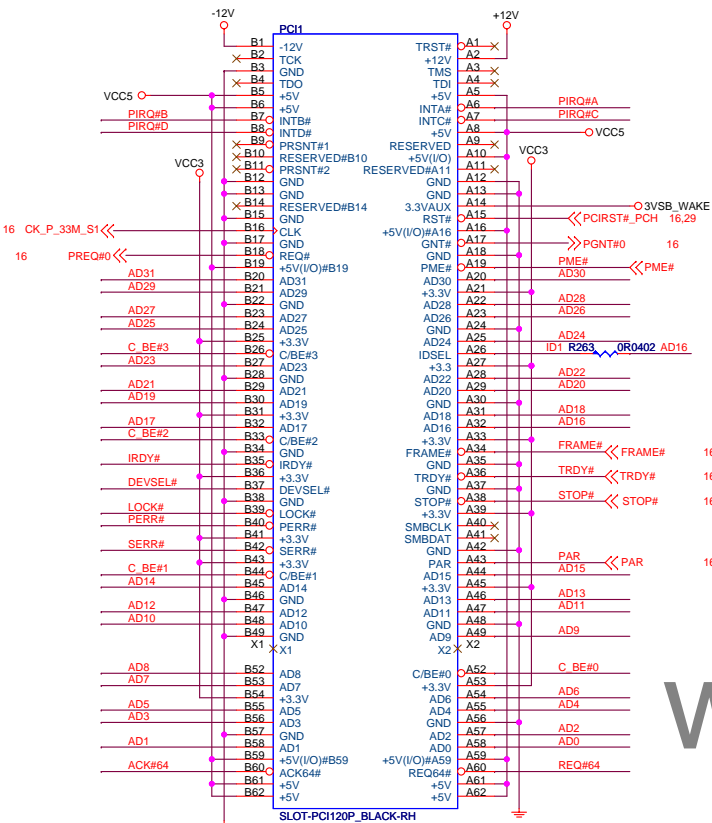
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



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MS-7681		
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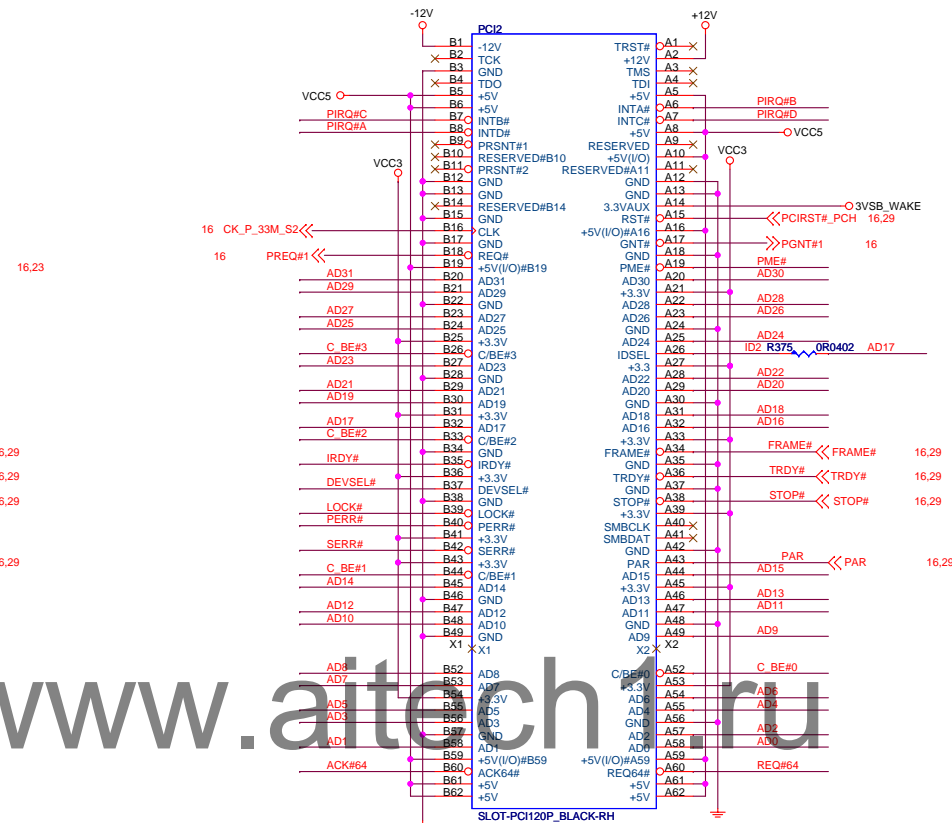
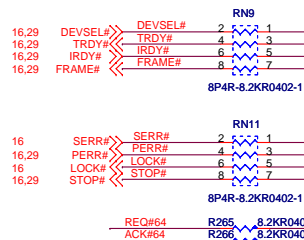
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

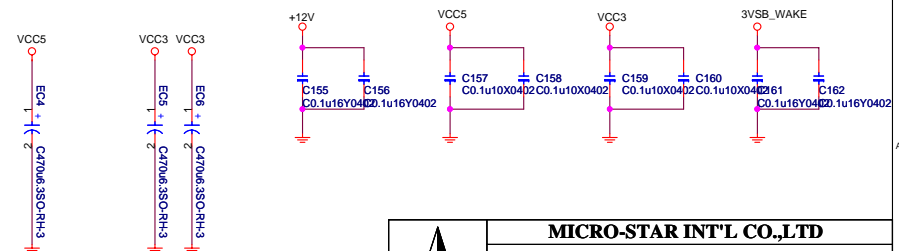
16,29 AD[31..0] << AD[31..0]
16,29 C_BE[3..0] << C_BE[3..0]

PCI PULL-UP / DOWN RESISTORS



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

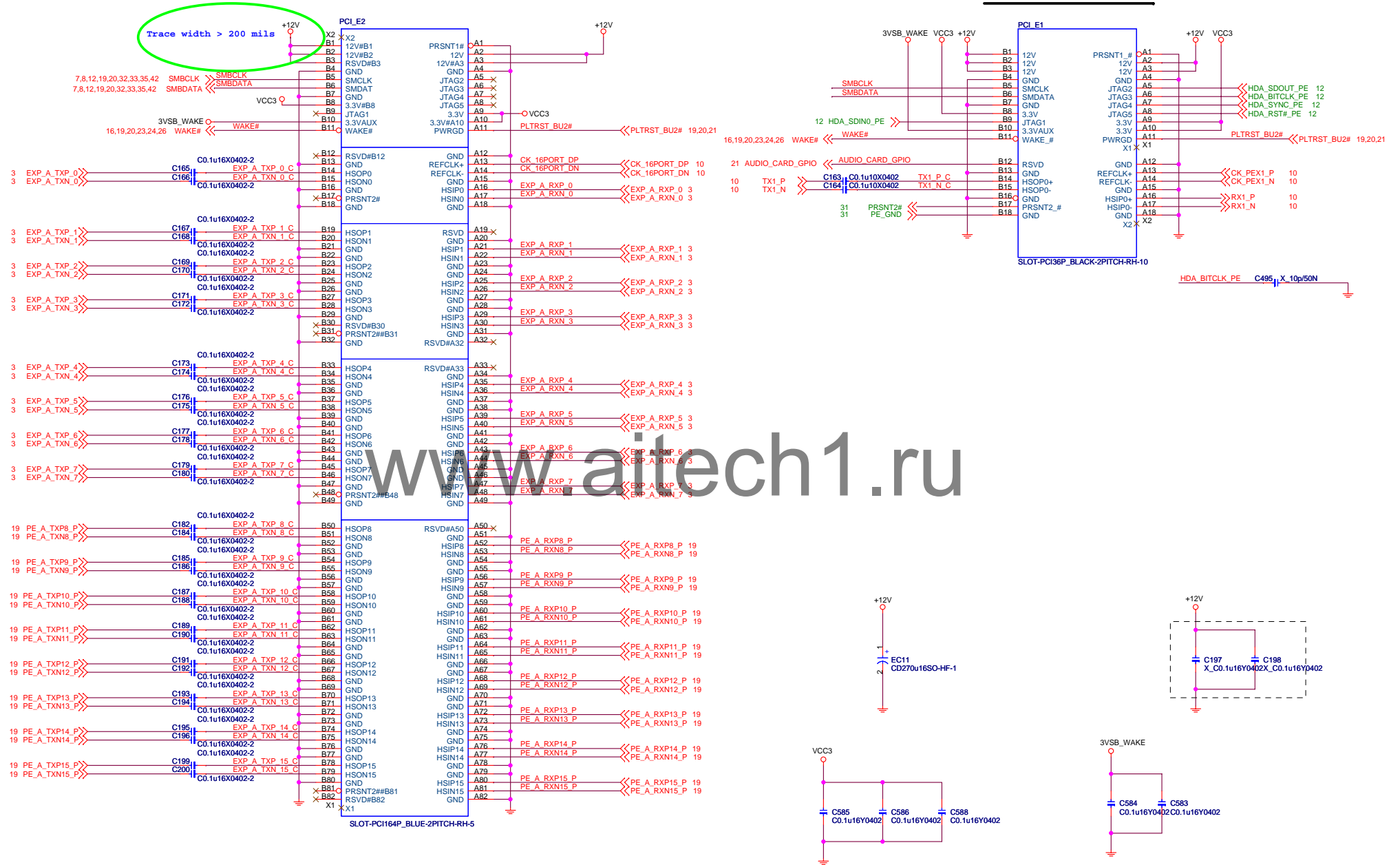
PCI SLOT DECOUPLING CAPACITORS



PCI_Express X16 Slot

HDA co-lay PCIe x1

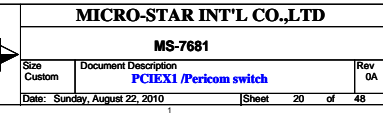
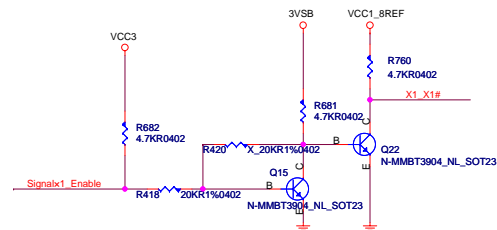
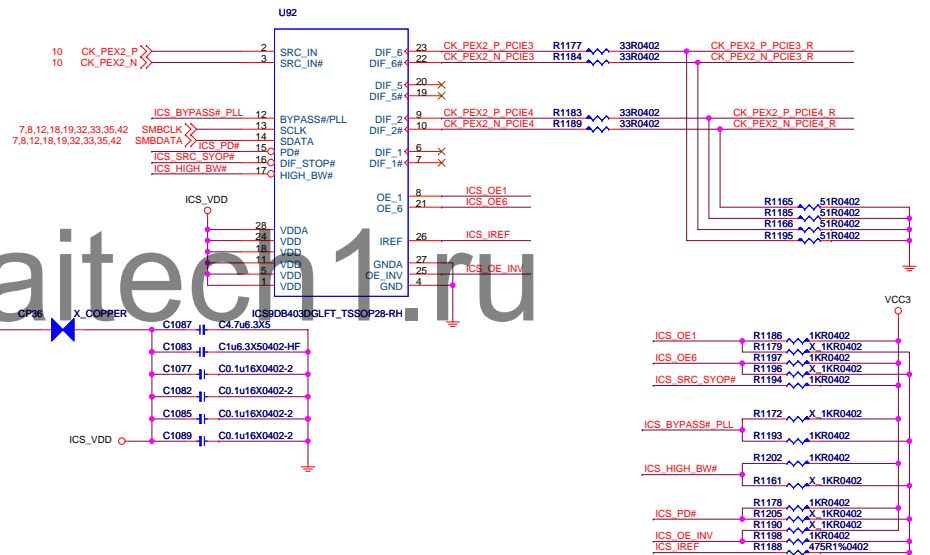
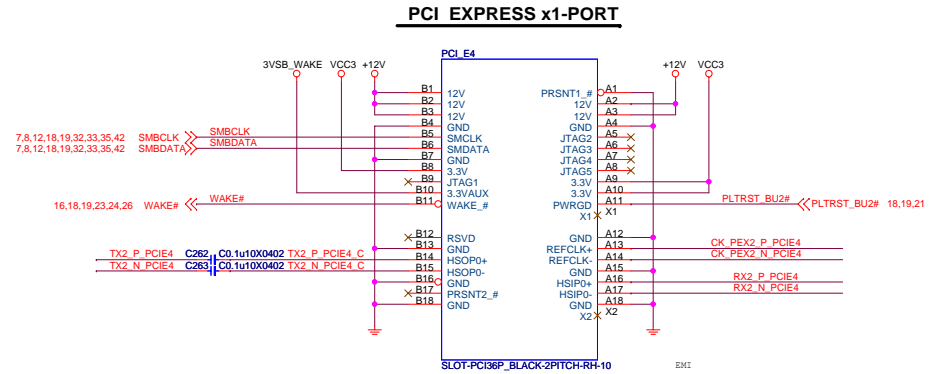
PCI EXPRESS x1-PORT

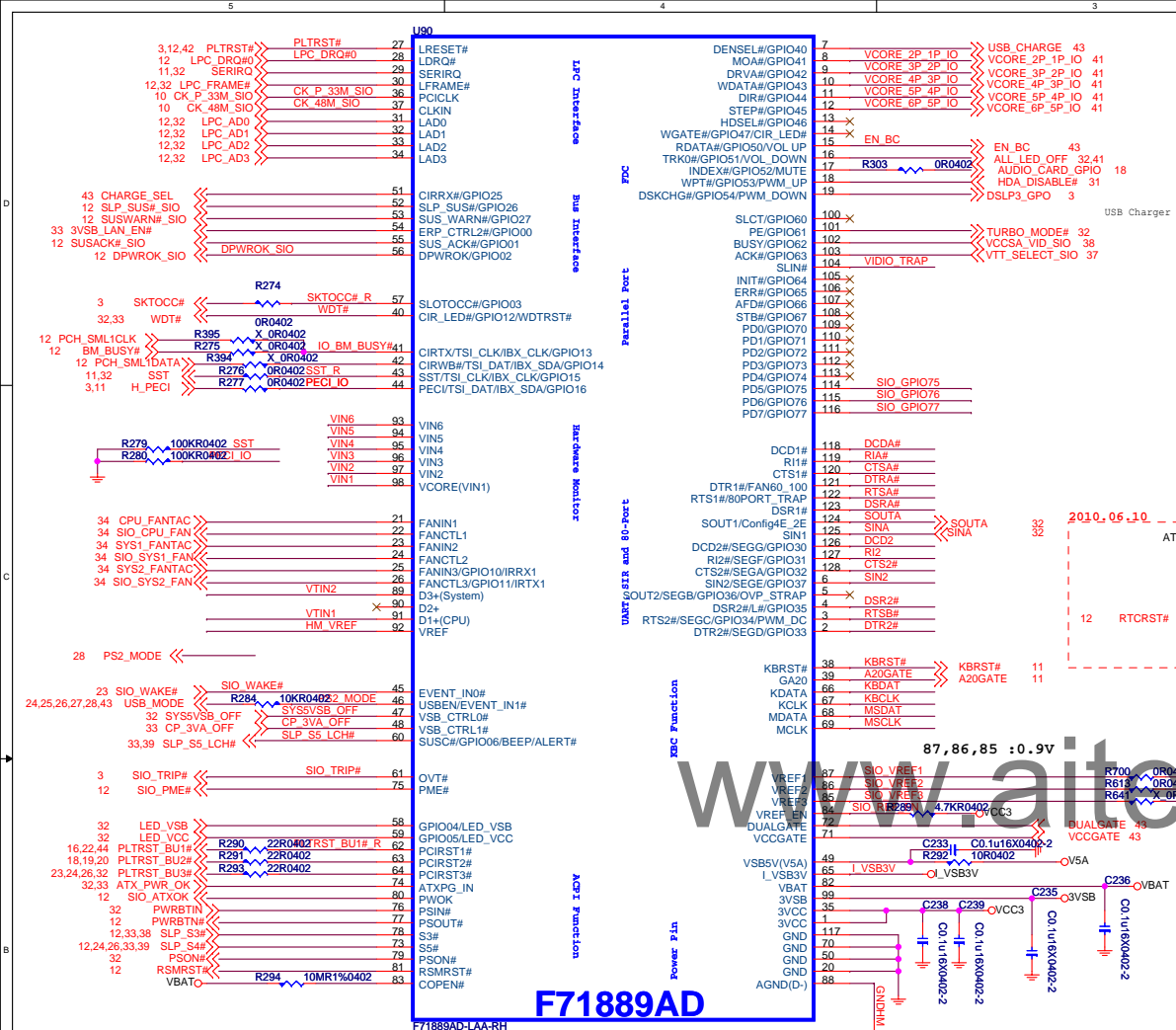


Trace width > 200 mils



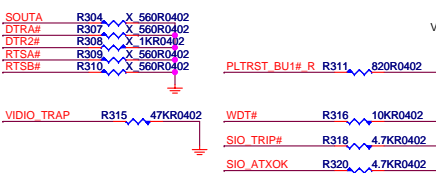
Size Custom	Document Description PCIEx8/Pericom switch	Rev 0A
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LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2#	PIN51~56=GPIO	PIN51~56=BUS
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port ENABLE	80 Port DISABLE
SLIN#	PD 47K, pin 100-103 and pin105-116 as GPIO pin.	

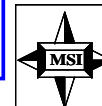
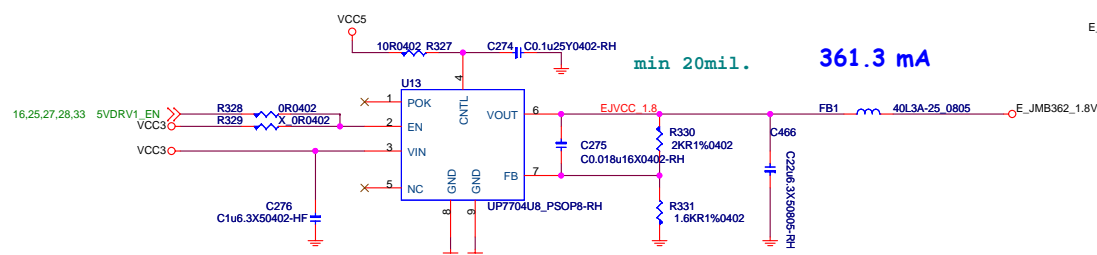


Pin4 and Pin9 over 20mil
1/7/10 update.



The image contains three circuit diagrams illustrating capacitor placement for various pins:

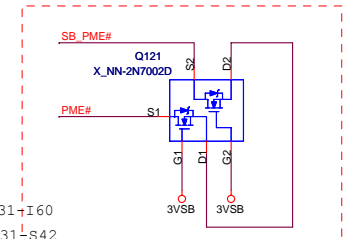
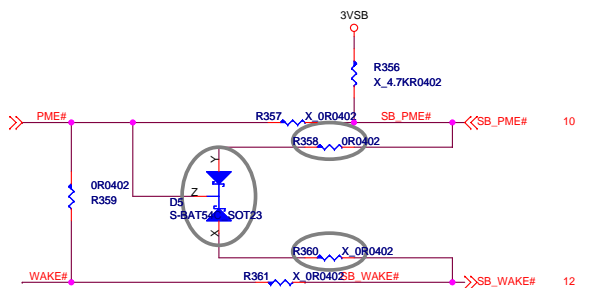
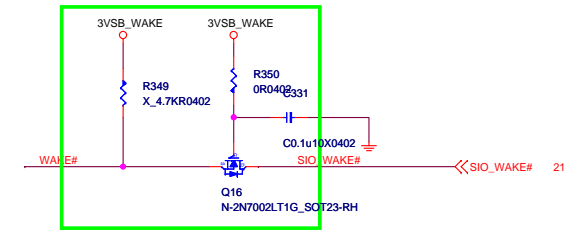
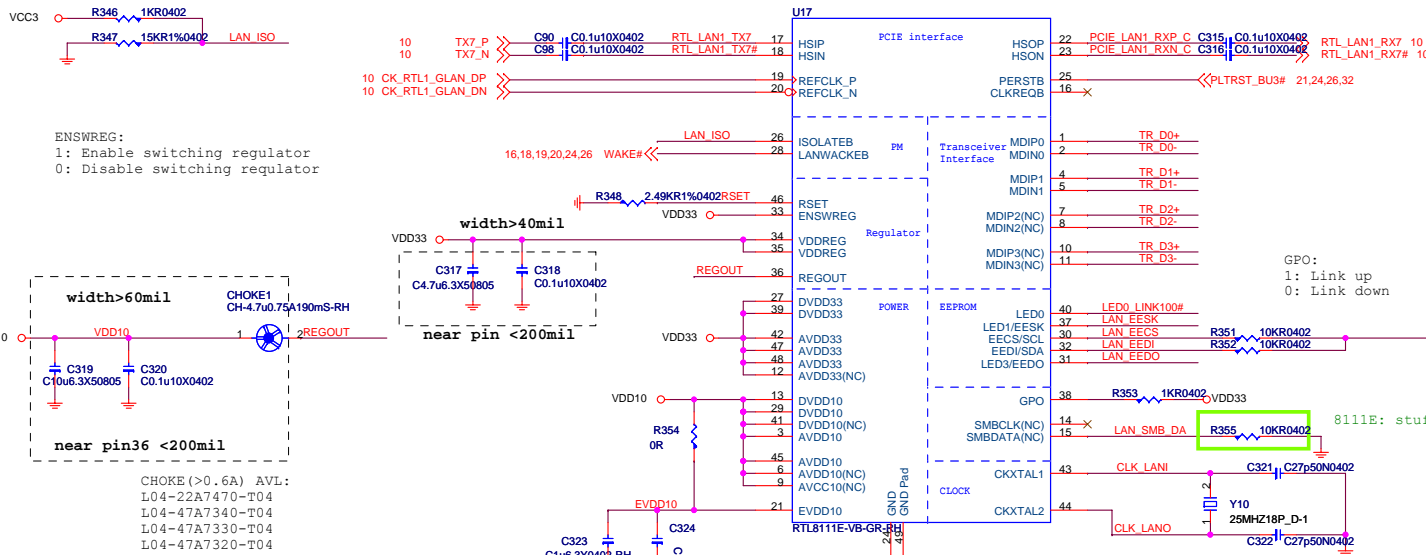
- Diagram 1 (Top Left):** A blue box highlights the area "near the pin 4". It shows a circuit connected to $E_JMB362_1.8V$. Three capacitors are connected to ground: C937 (10u/10V/8), C936 (0.1u/25V/4), and C921 (102P/50V/4).
- Diagram 2 (Top Right):** Shows a circuit connected to $VCC3$. Three capacitors are connected to ground: C932 (0.1u/25V/4), C933 (0.1u/25V/4), and C913 (0.1u/25V/4). The text "near the pin 16,32,44" is written above the capacitors.
- Diagram 3 (Bottom Left):** Shows a circuit connected to $E_JMB362_1.8V$. Four capacitors are connected to ground: C914 (0.1u/25V/4), C918 (0.1u/25V/4), C912 (0.1u/25V/4), and C923 (0.1u/25V/4). The text "near the pin 1,13,33,41" is written above the capacitors.
- Diagram 4 (Bottom Right):** A blue box highlights the area "near the pin 9". It shows a circuit connected to ground. Four capacitors are connected to ground: C922 (0.1u/25V/4), C931 (0.1u/25V/4), C928 (X_10u/10V/8), and C911 (0.1u/25V/4). The text "near the pin 21,27" is written above the first two capacitors.



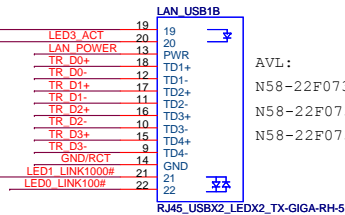
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MS-7681			
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RTL8111E Giga LAN

LAN/PCIE/PCI Wake Up CTRL Circuit



LAN Connector

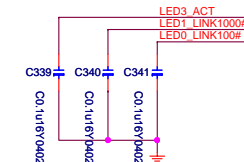
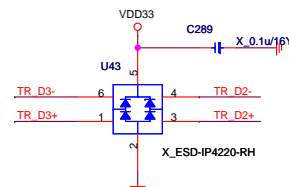
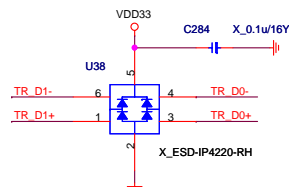


AVL:
N58-22F0731-I60
N58-22F0731-S42
N58-22F0731-U30

Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22

8111E POWER Consumption

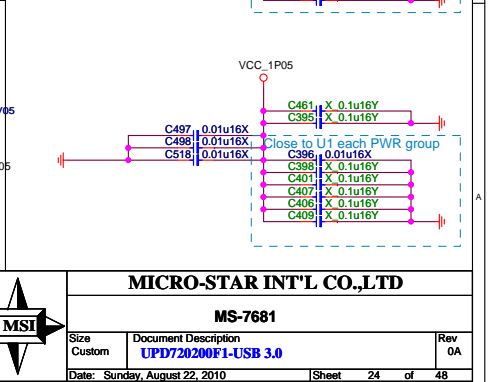
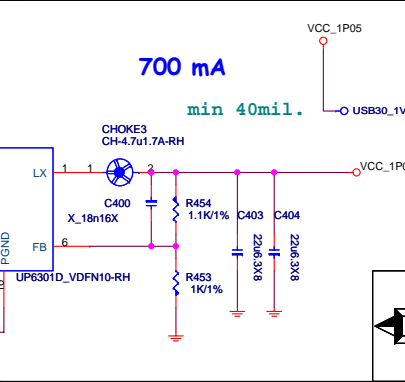
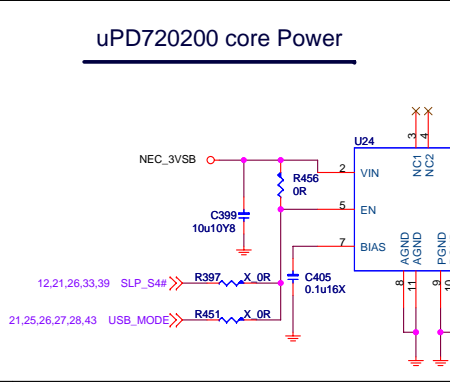
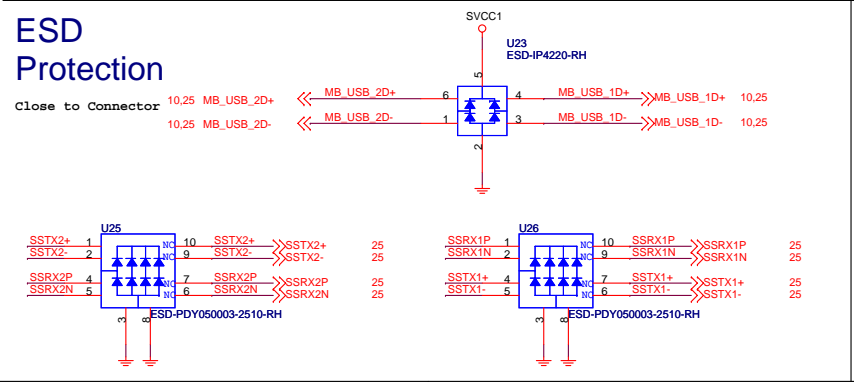
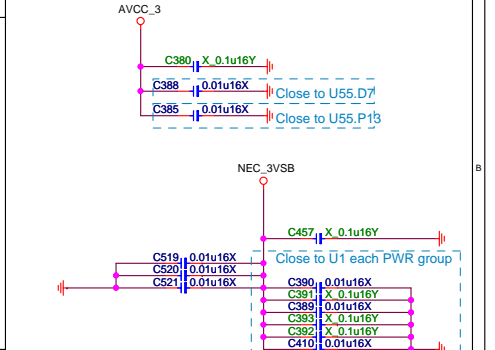
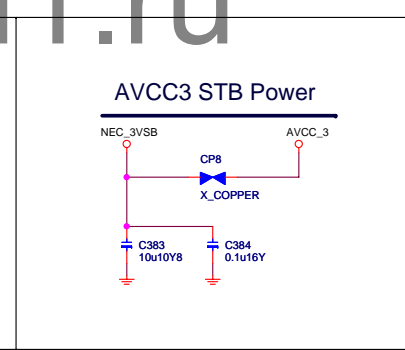
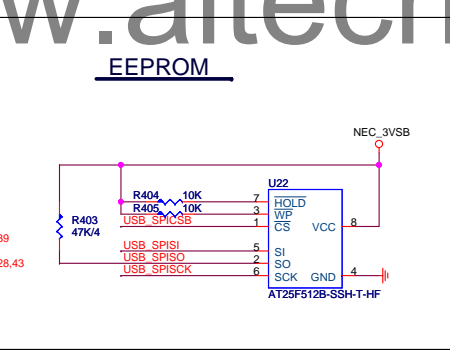
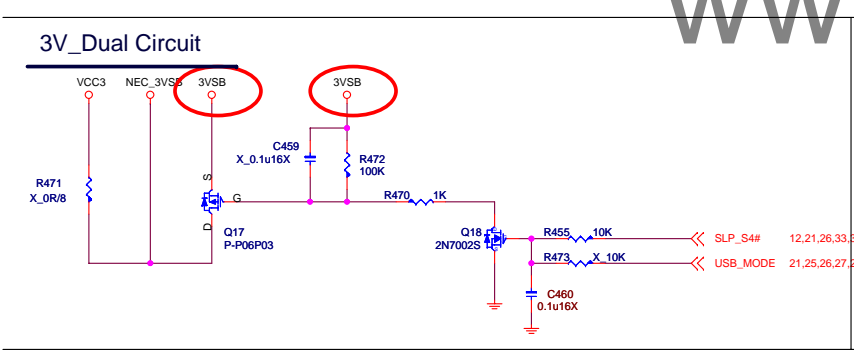
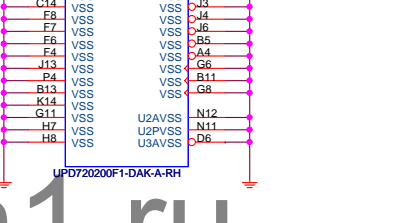
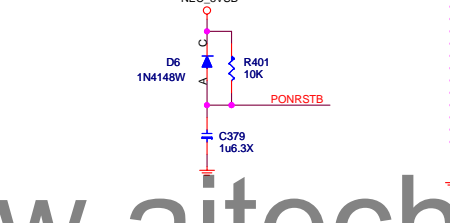
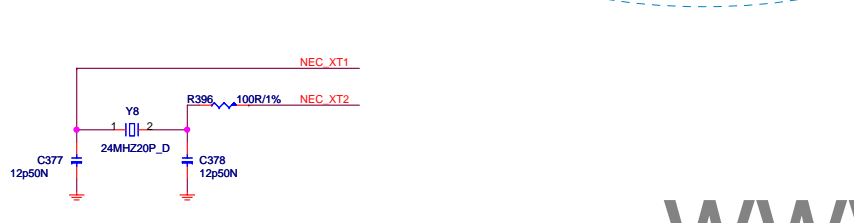
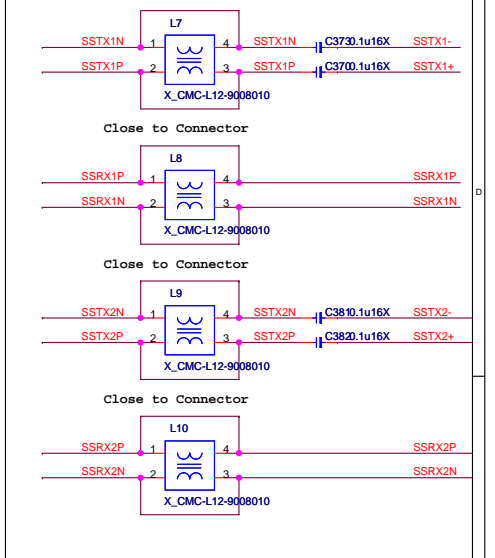
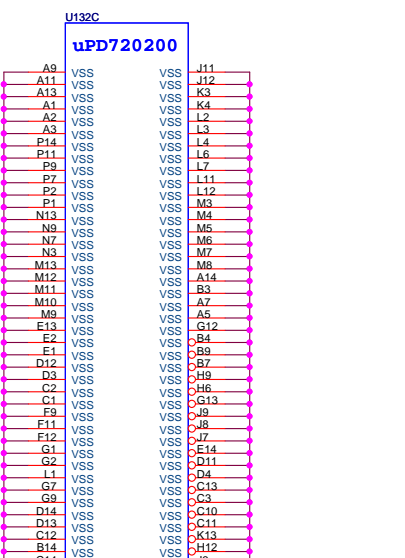
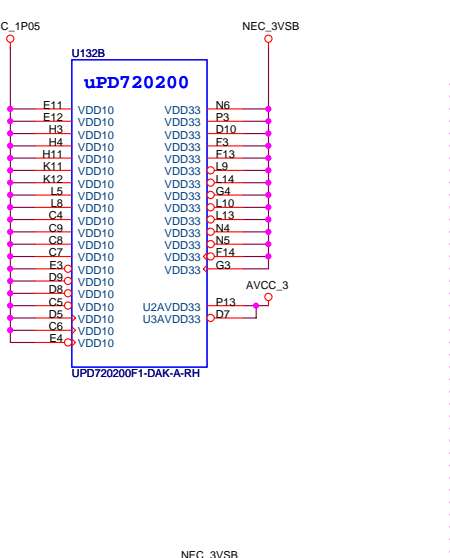
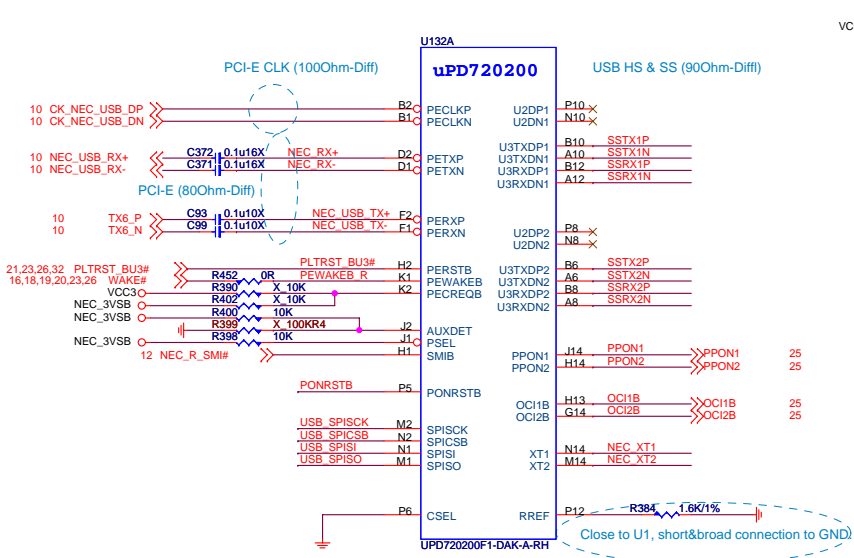
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

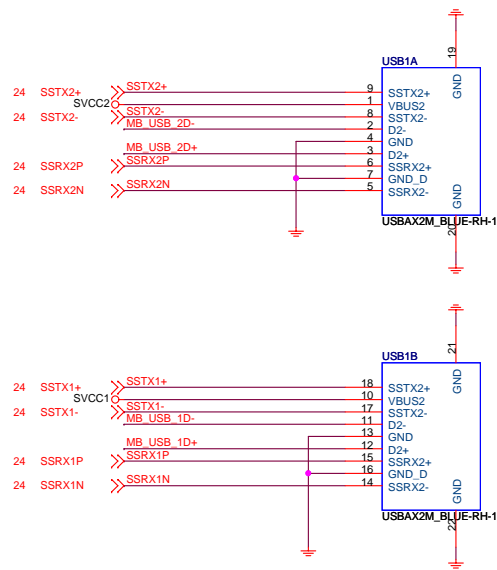


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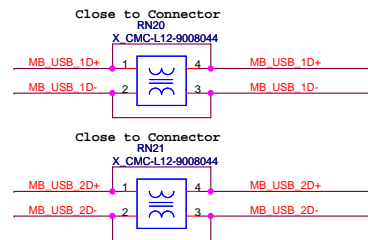
MS-7681

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Custom	LAN-RTL8111E-1	0A
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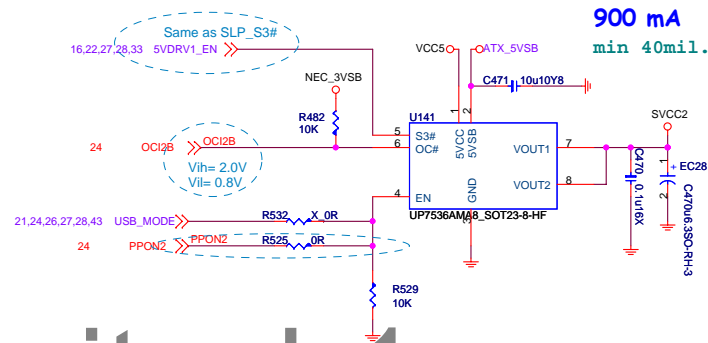
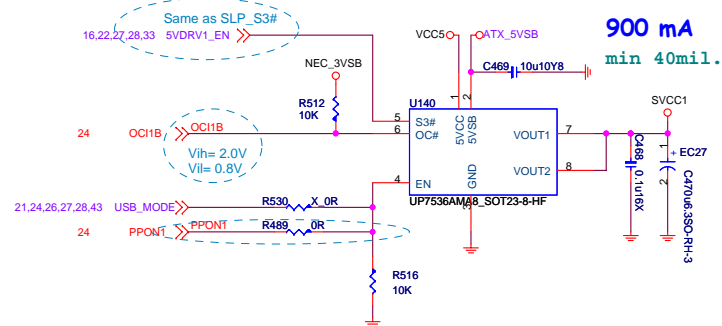




10,24 MB_USB_1D+ >>>
 10,24 MB_USB_1D- >>>
 10,24 MB_USB_2D+ >>>
 10,24 MB_USB_2D- >>>

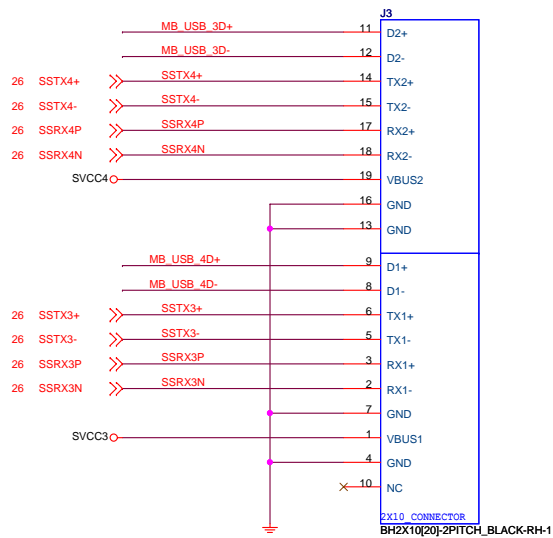


All power sources of uPD720200 are supplied, PPN0x is enable.
 PPN0x is low when OC0x going to low.

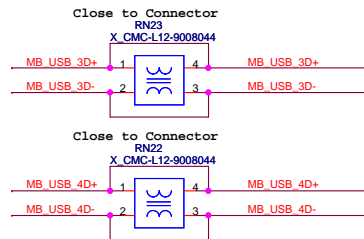
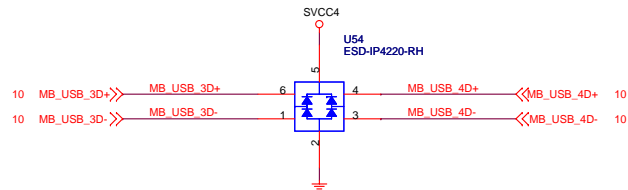
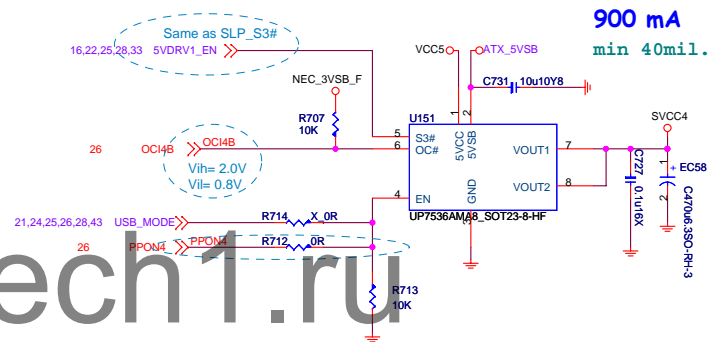
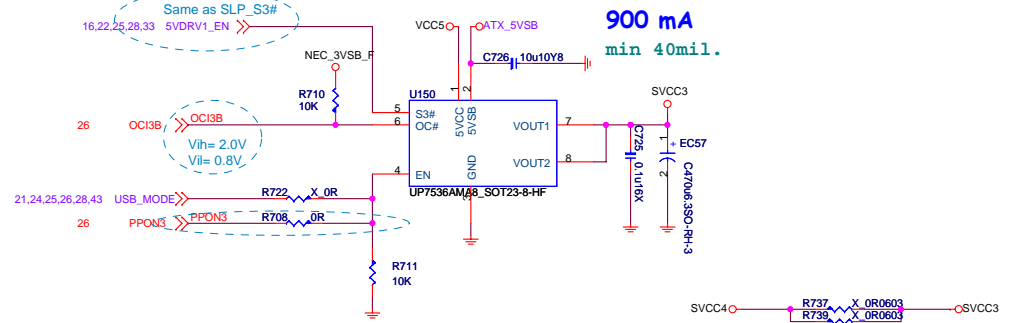


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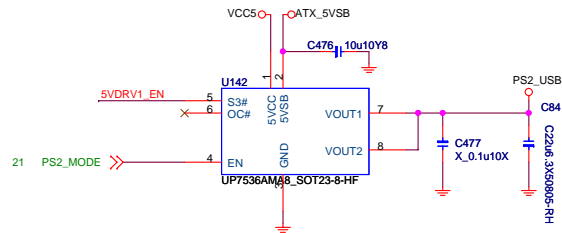


All power sources of uPD720200 are supplied, PPN0x is enable.
PPN0x is low when OC1x going to low.



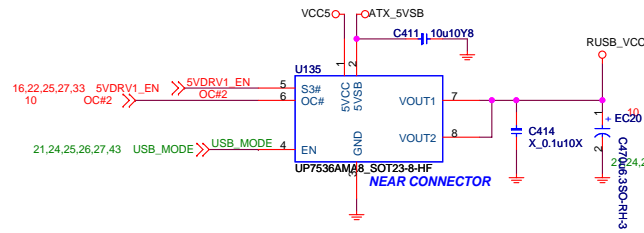
Front USB Connector

USB POWER FOR PORT 11,12

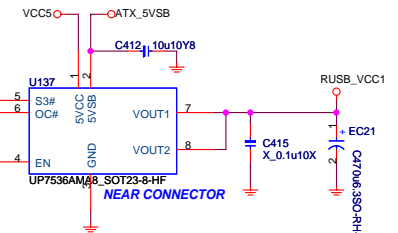


Rear USB Connector

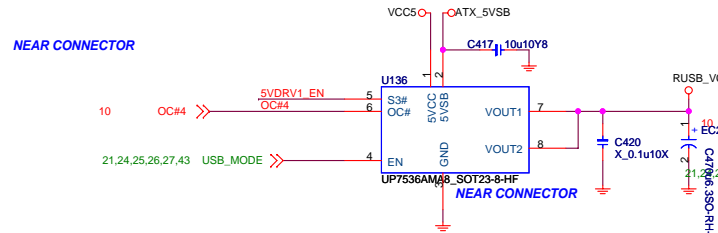
USB POWER FOR PORT 4,5



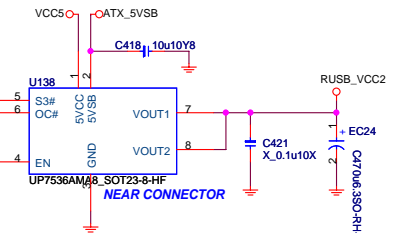
USB POWER FOR PORT 6,7



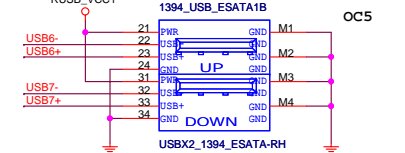
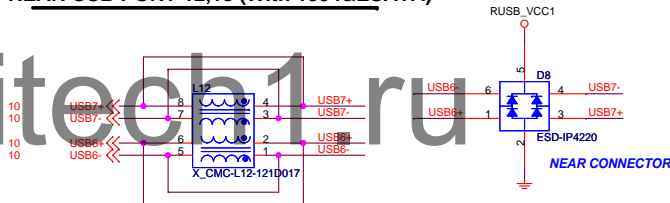
USB POWER FOR PORT 11,12



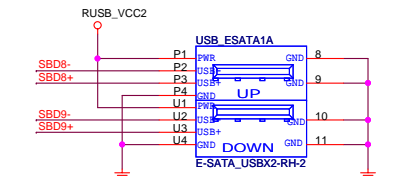
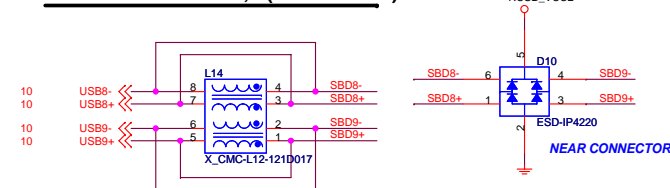
USB POWER FOR PORT 8,9



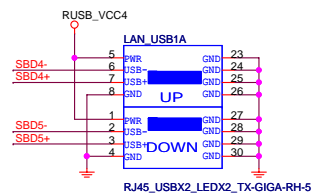
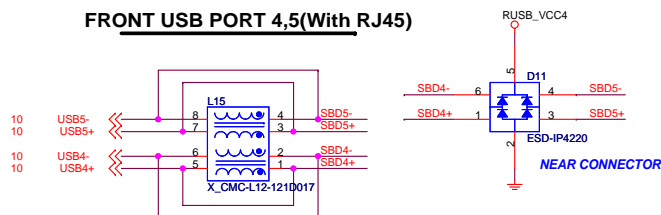
REAR USB PORT 12,13 (With 1394&ESATA)



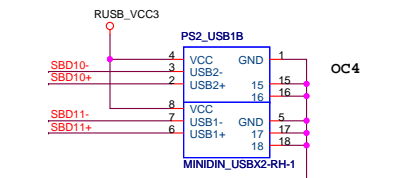
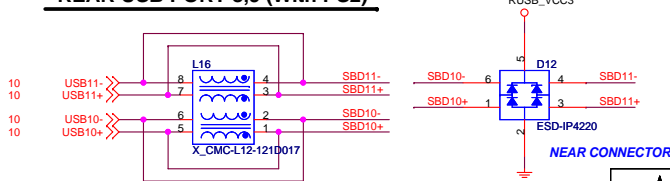
REAR USB PORT 8,9 (With ESATA)



FRONT USB PORT 4,5(With RJ45)



REAR USB PORT 8,9 (With PS2)



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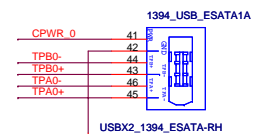
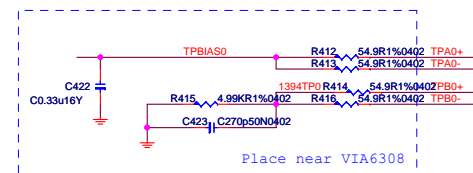
VT6308P - 1394 Controller

Trace Width/Spceing: 4/10/4

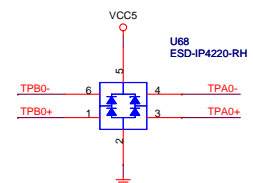
Impedance: 110 Ω / ± 6

Trace Length: < 6"

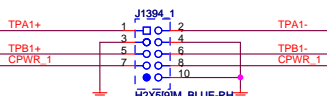
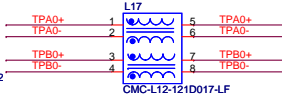
Rear 1394 port



USBX2_1394_ESATA-RH

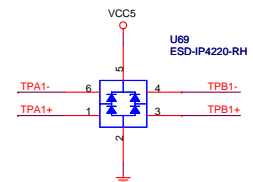
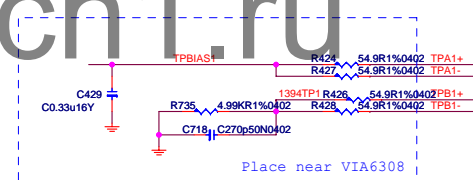


Close to Connector

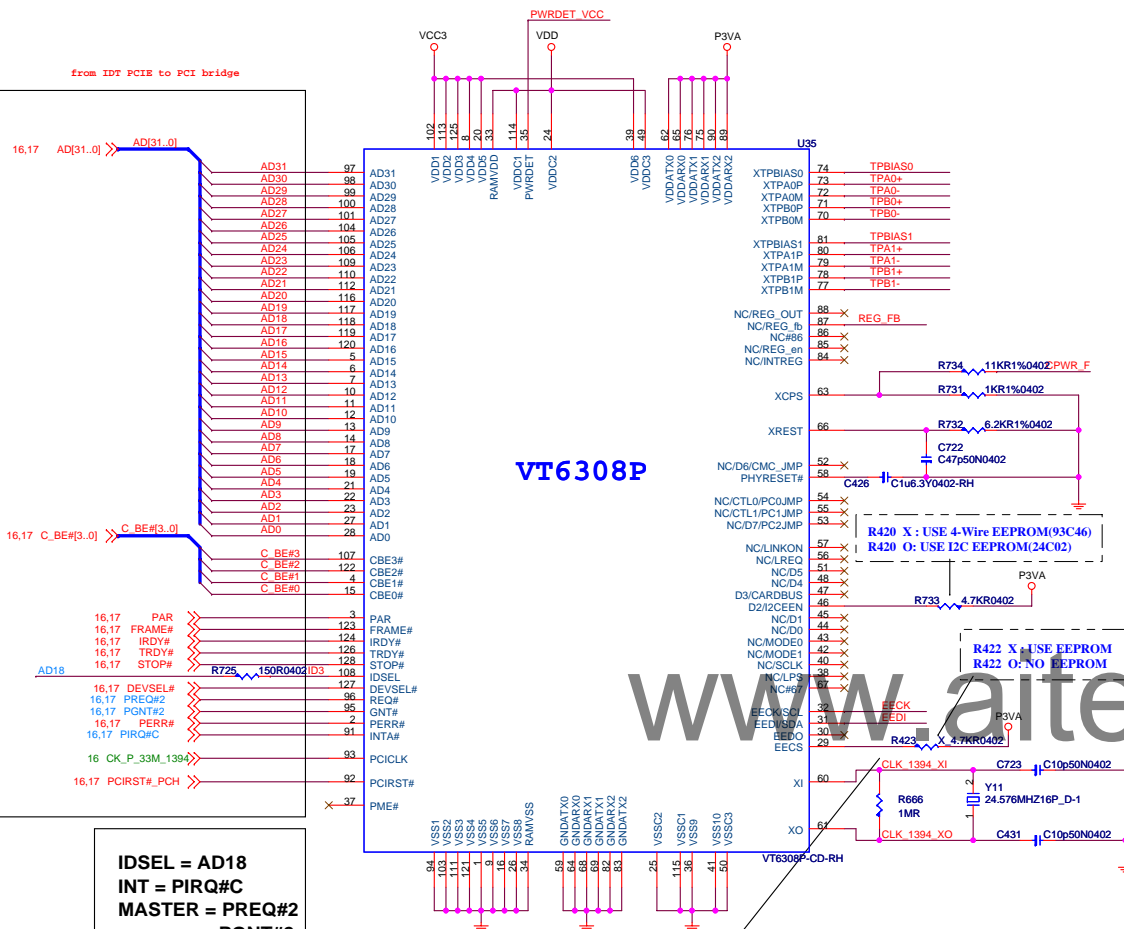
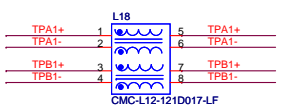


For Intel 1394 pinheader

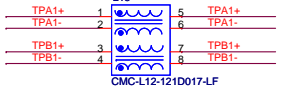
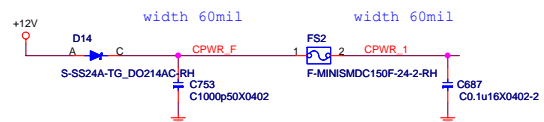
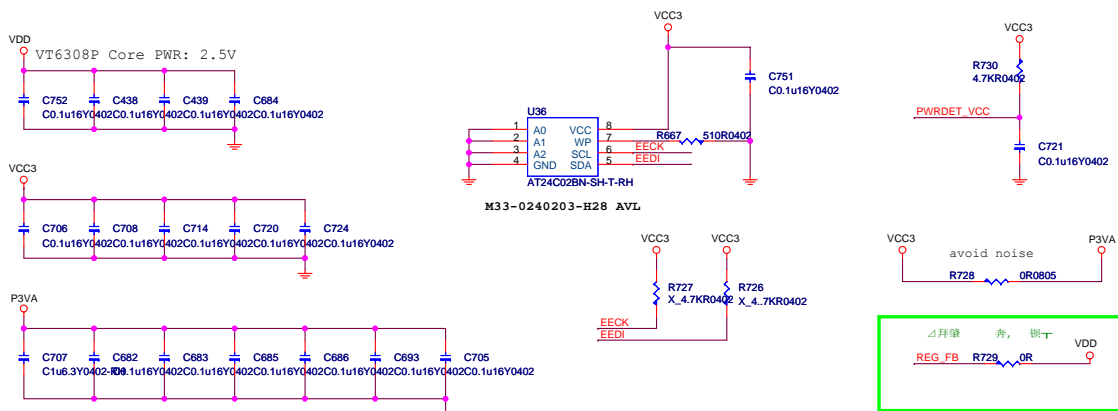
Front 1394 pin header



Close to Connector



```
IDSEL = AD18
INT = PIRQ#C
MASTER = PREQ#2
PGNT#2
```



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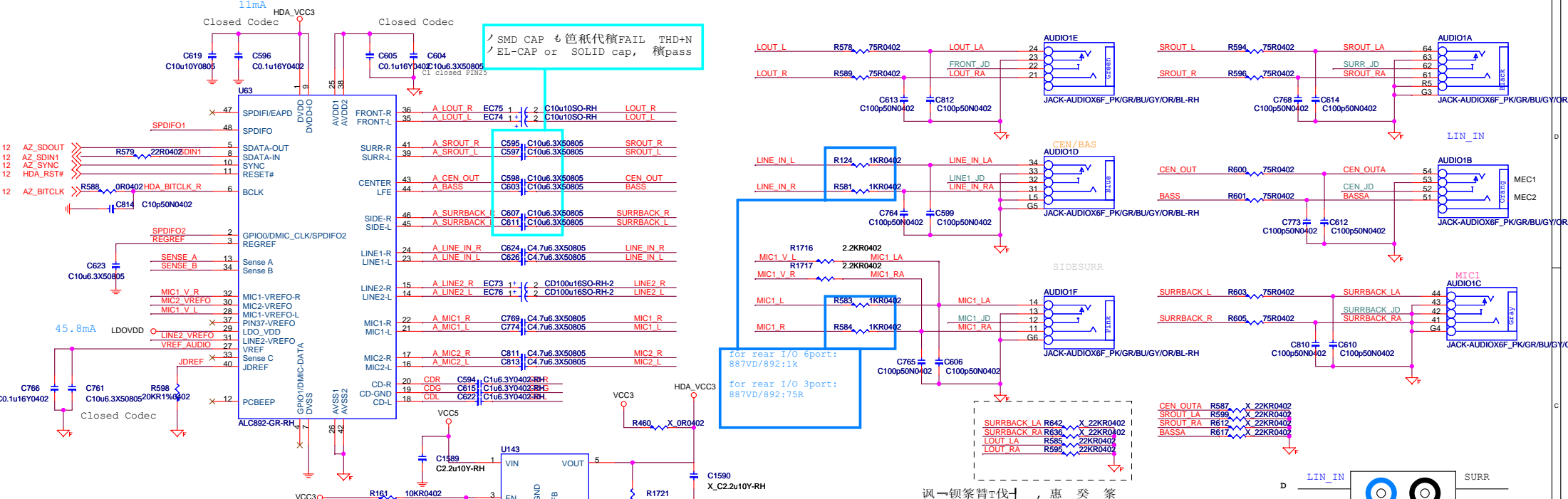
MS-7681

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Rev	0A
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Date: Sunday, August 22, 2010

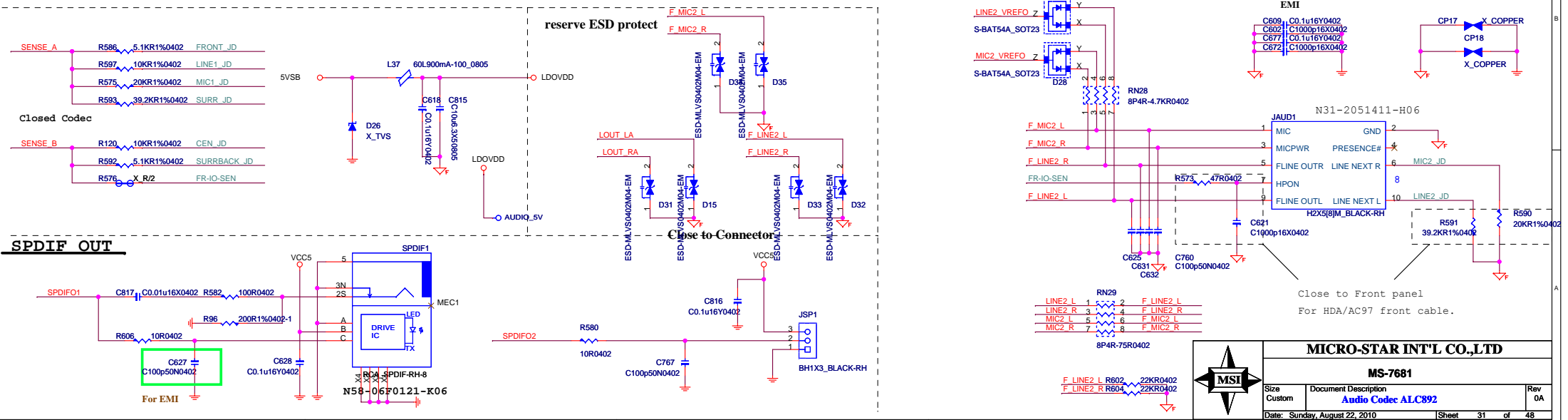
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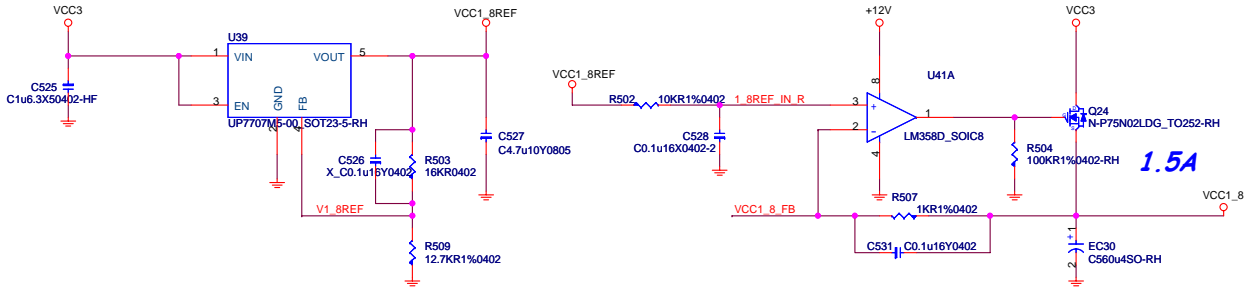
	PRSN2#	PE_GND
Other card	0	0
4132 audio	1	0
N/A	1	NC

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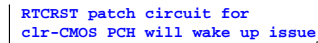
to SIO GPI pin
Hi: onboard codec Verb table
Low: PCIE Audio Verb table
disable onboard codec by H/W
Stuff: U18, Q40, R132, Unstuff: R439
disable onboard codec by BIOS
Unstuff: U18, Q40, R132; tuff: R439



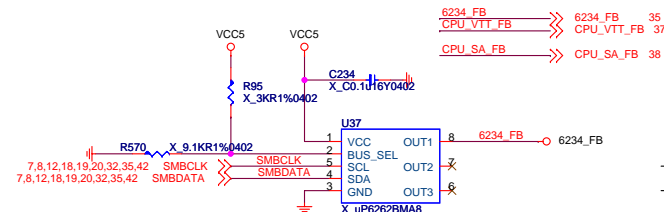
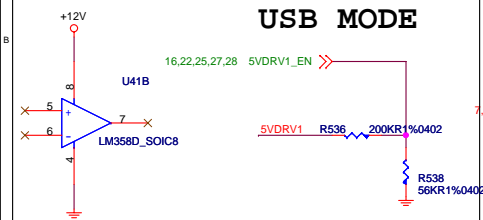
VCC1_8REF



3VSB

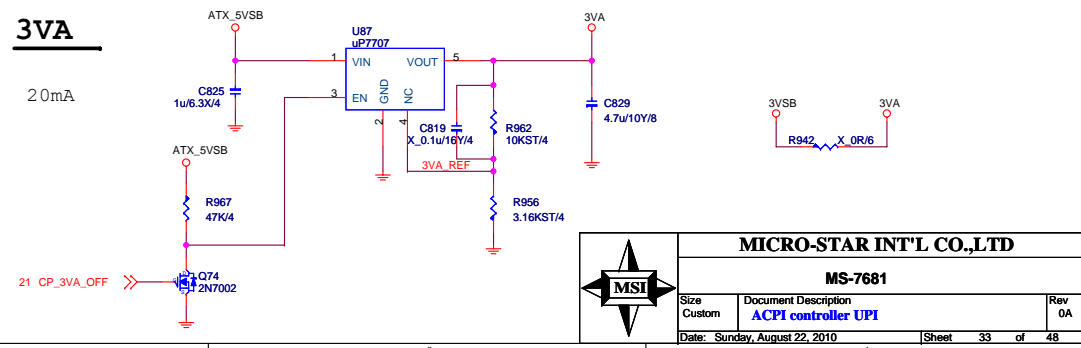


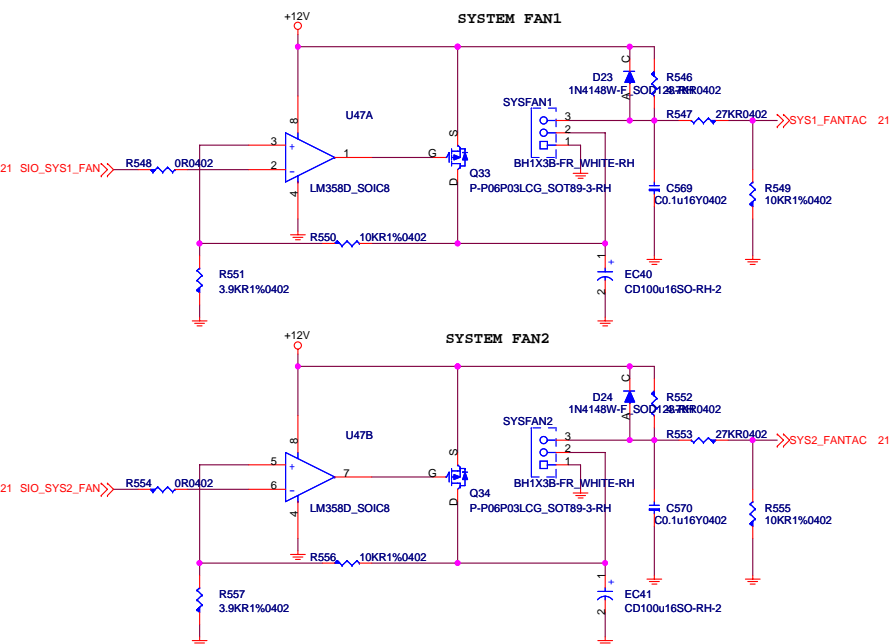
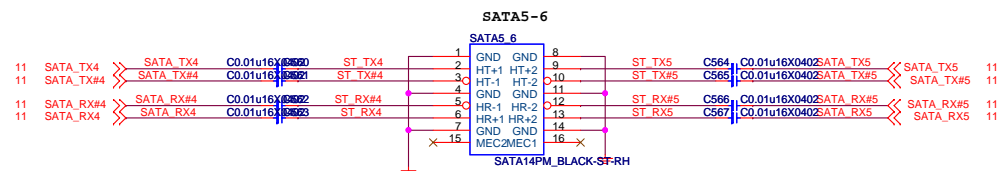
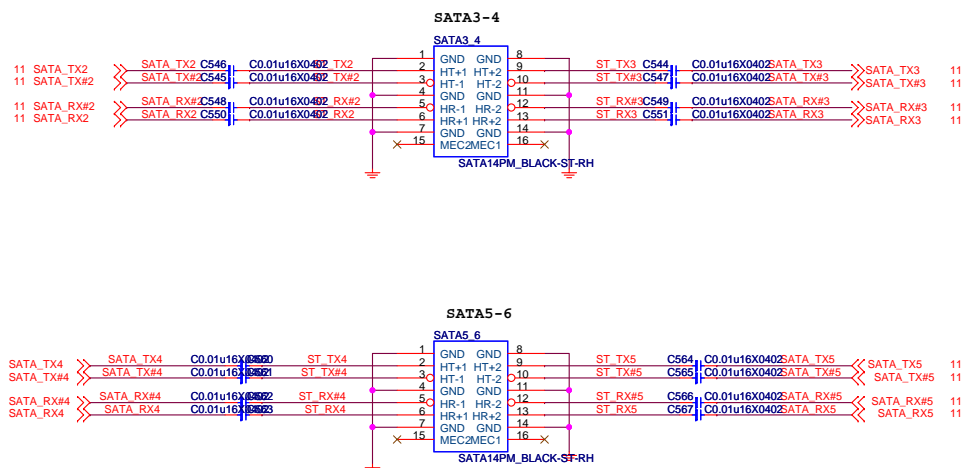
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0x20:RH=10K,RL=OPEN

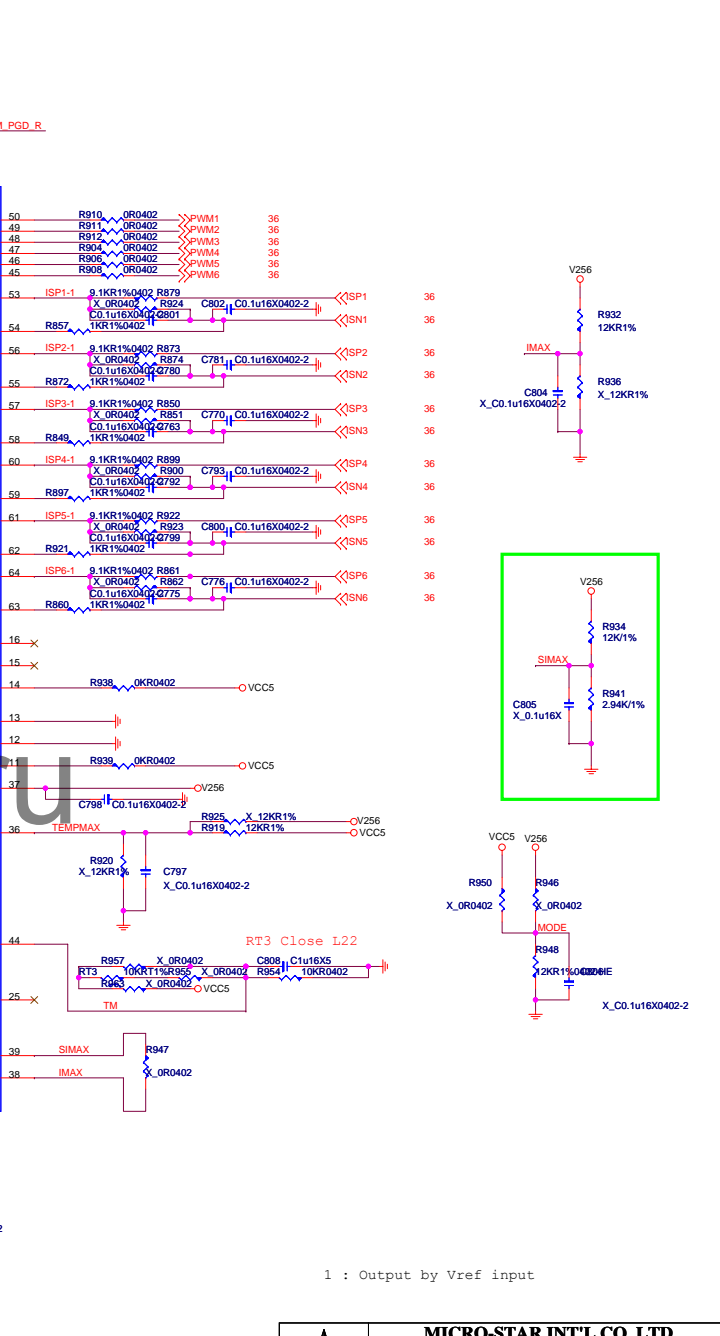
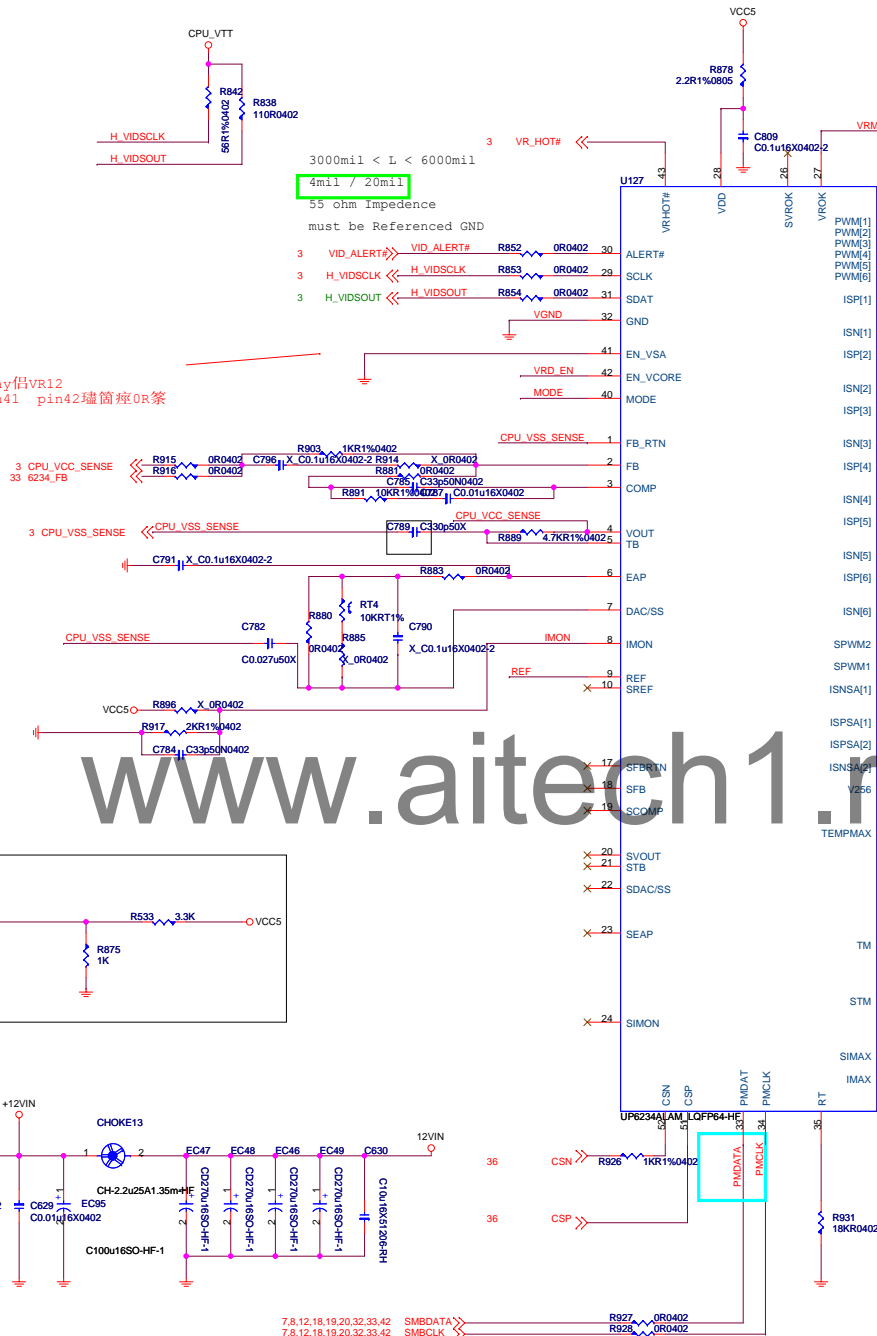
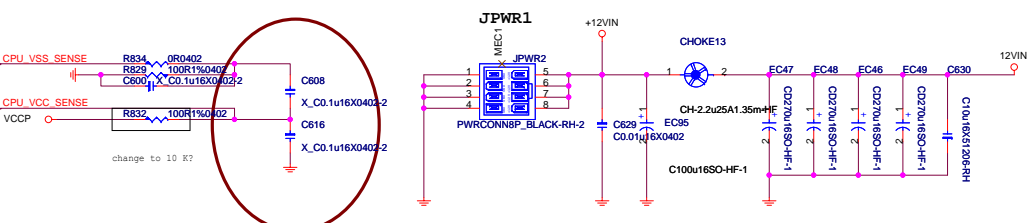
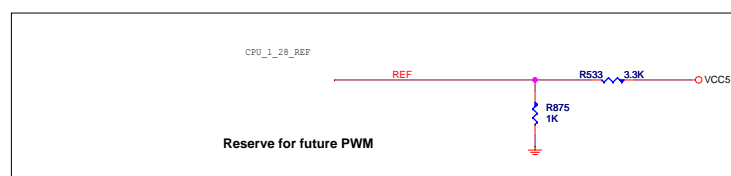
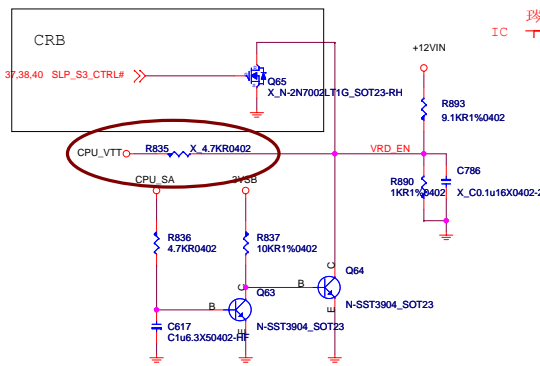
20mA





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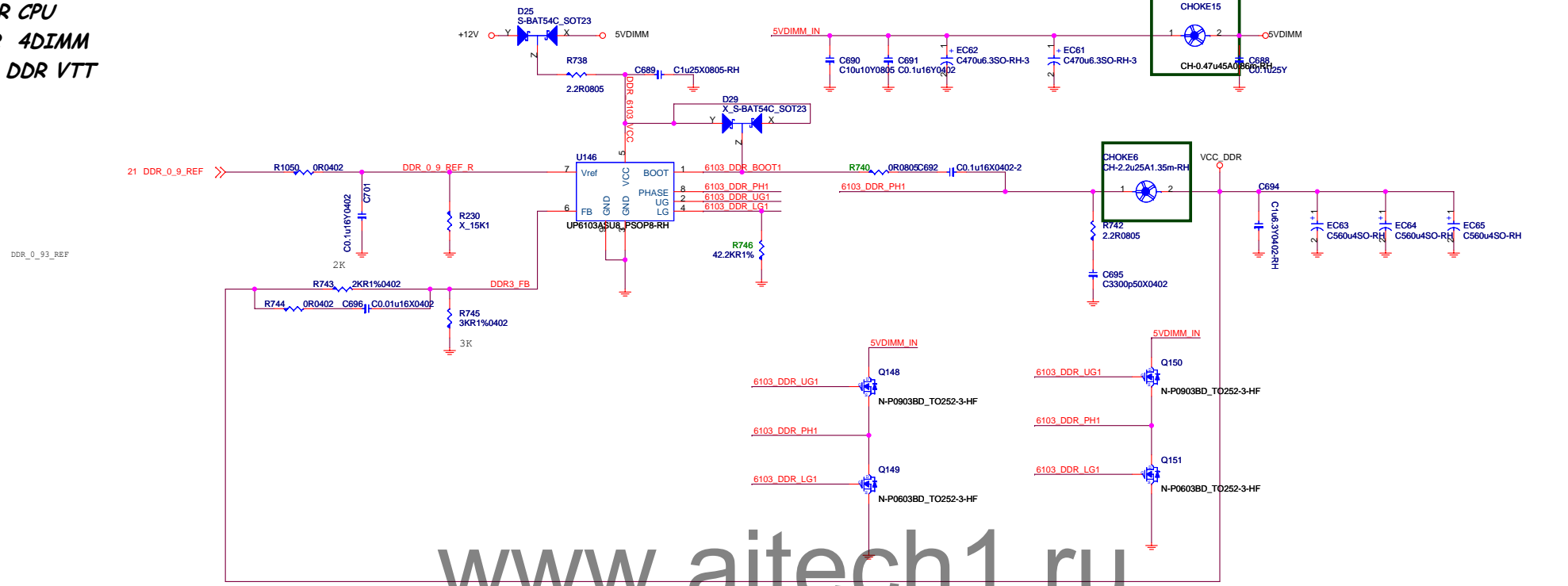
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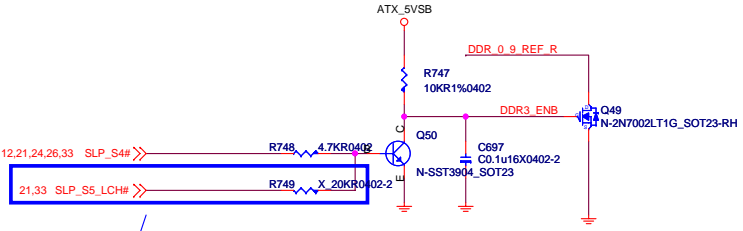
DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

$I_{ripple}=7.7A$
 $4.7*2=9.4A>7.7A$

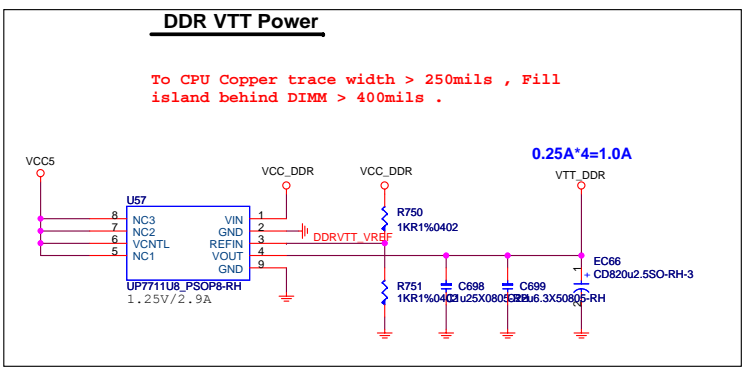


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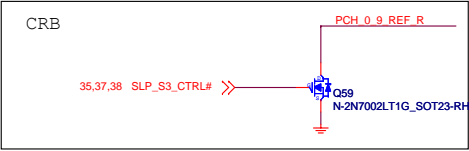
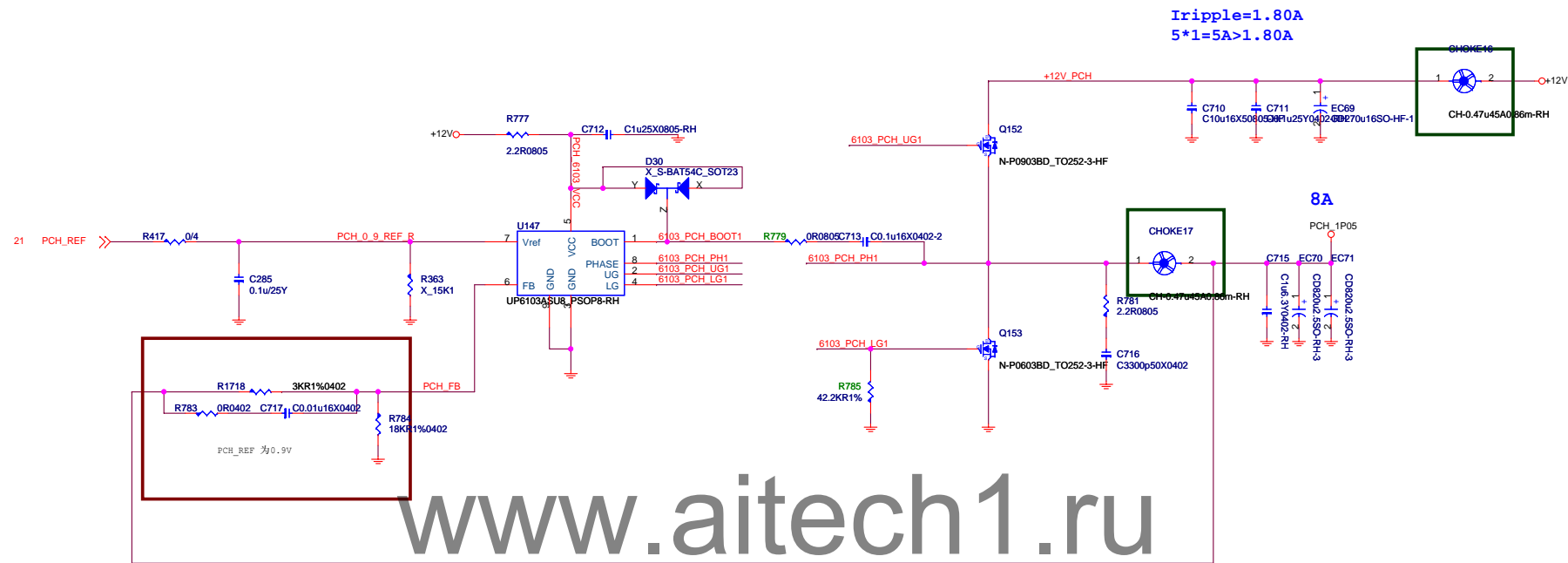


Meet Intel Power Down Sequence

If you use LAA and can support deep_s3,
please use SLP_S5_LCH#, else use SLP_S4#.



PCH Core 6.2A+1.8A=8A



	uP6103A	uP6138
PIN1	BOOT	BOOT
PIN2	UG	UG
PIN3	GND	VREFIN
PIN4	LG	LG
PIN5	VCC	VCC
PIN6	FB	FB
PIN7	Vref	OCF/EN
PIN8	PHASE	PHASE
PIN9	GND	GND

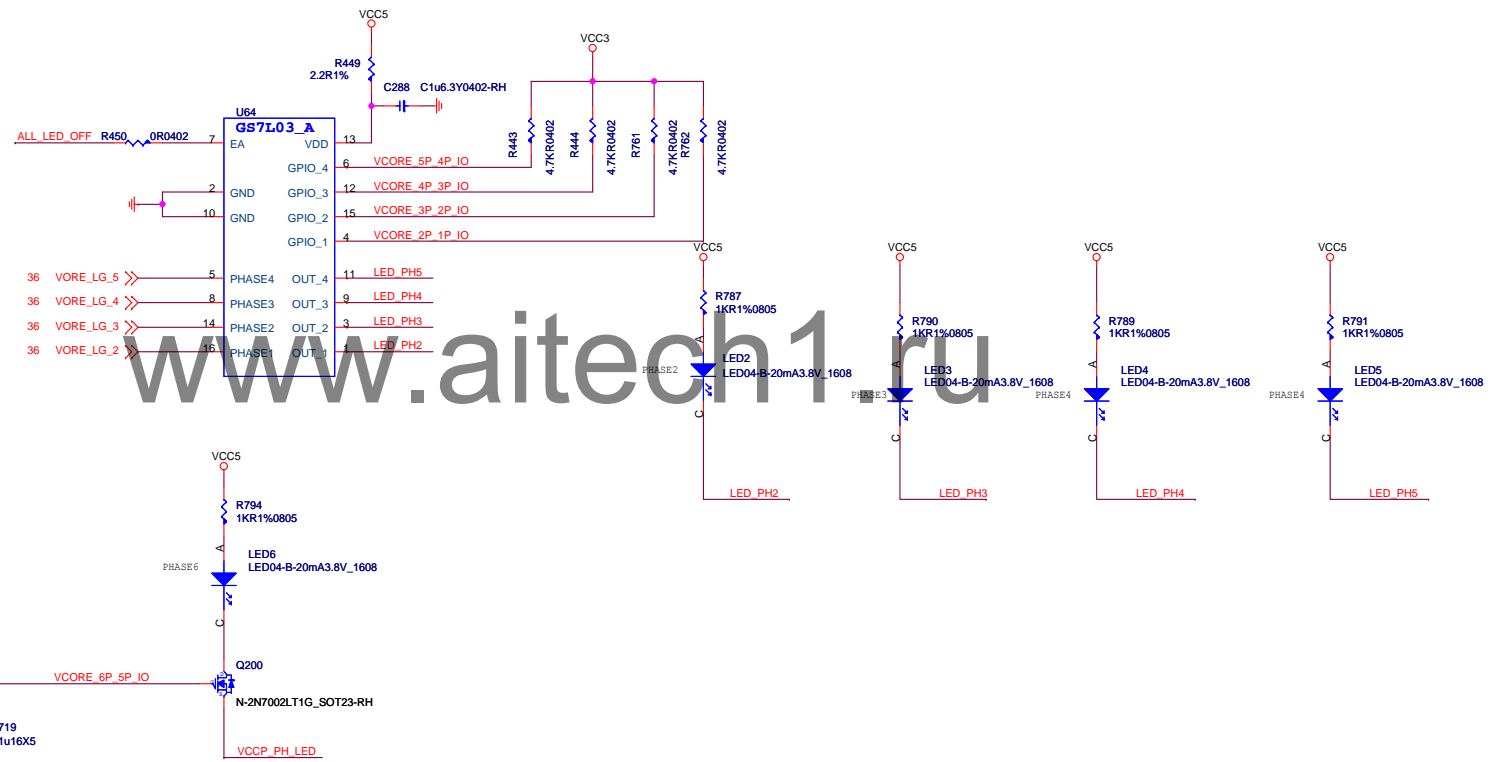
21 VCORE_5P_4P_IO>> VCORE_5P_4P_IO

21 VCORE_4P_3P_IO>> VCORE_4P_3P_IO

21 VCORE_3P_2P_IO>> VCORE_3P_2P_IO

21 VCORE_2P_1P_IO>> VCORE_2P_1P_IO

21,32 ALL_LED_OFF >> ALL_LED_OFF
原來是ALL_LED_OFF#，



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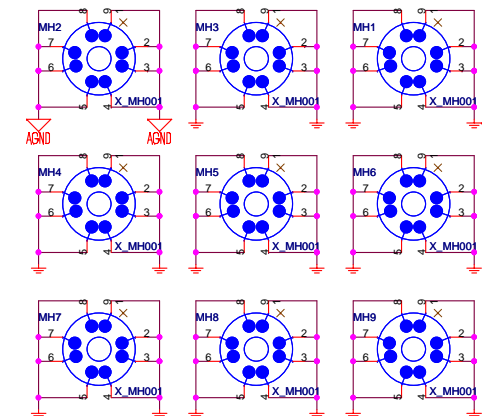
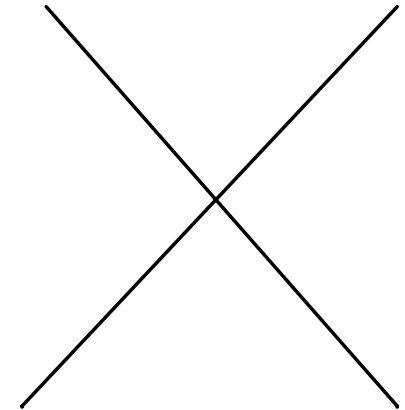
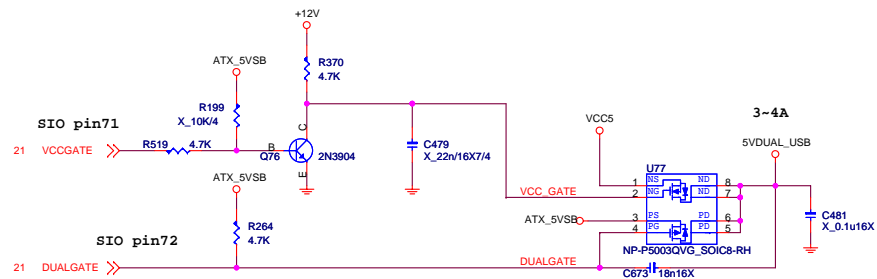


Diagram illustrating the HS-0404592-RH component assembly. The assembly consists of a main component (HS-0404592-RH) connected to a U4_X1 component. The main component is a rectangular block with a blue star logo and the text "HS-0404592-RH". It is connected to the U4_X1 component via two orange wires. The U4_X1 component is a rectangular block with a blue star logo and the text "U4_X1". The diagram also shows a small component labeled "1" and "2" connected to the main component.

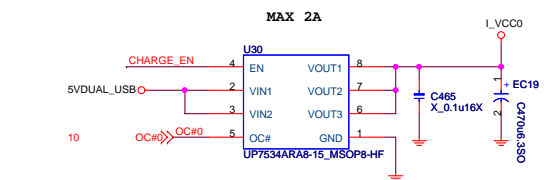


吹邻紅 (MSIS)
吹邻紅 (MSIS)

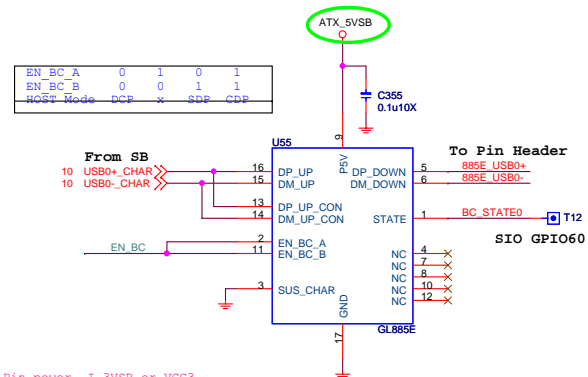
5VDUAL_USB



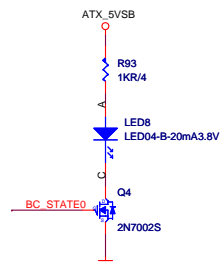
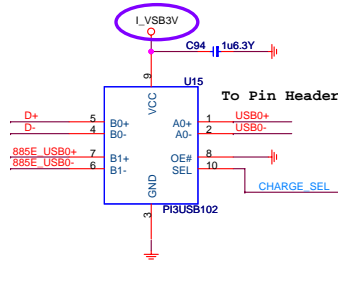
USB POWER FOR PORT 0 for Battery Charging



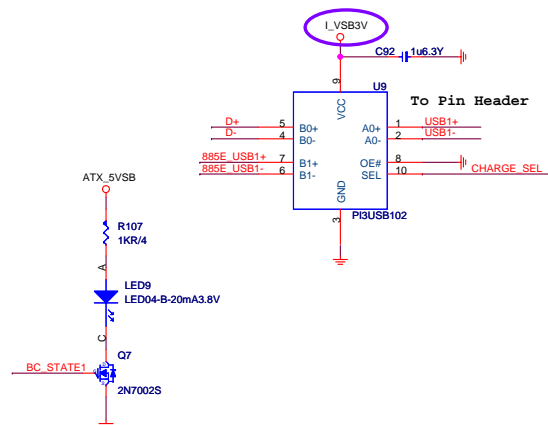
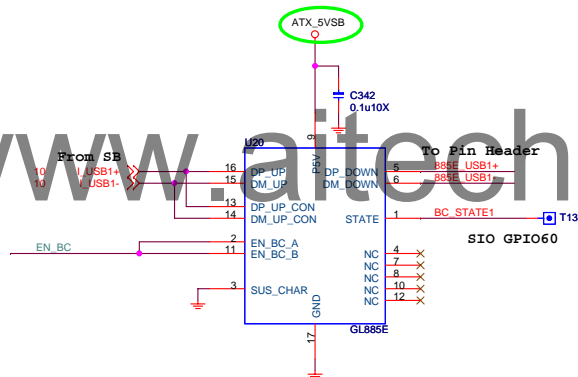
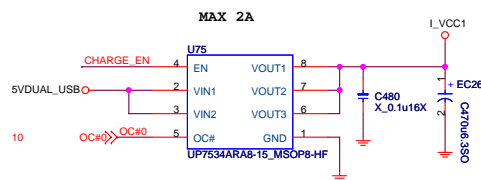
2010.06.08



Pin power I_3VSB or VCC3
Register power I_3VSB or VCC3
Register reset I_3VSB or LRESET#



USB POWER FOR PORT 1 for I charge



SIO GPIO40 Pin7 (VBAT for New F71889AD)

USB_CHARGE:

0: Don't support USB charge and resume.
1: Support USB charge and resume.

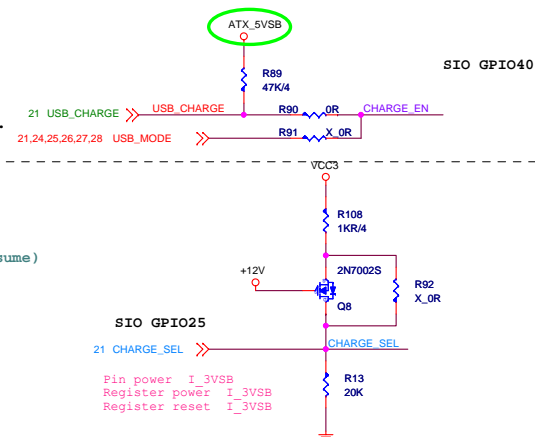
1st boot , H/W default support USB charge.

SIO GPIO50 (I_VSB3V)

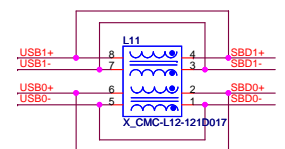
BC_SEL: (PUSH PULL)

```
0: Support DCP device(don't support usb link and resume)
1: Support CDP (Support usb link and resume)
```

1st boot , H/W default support DCP.

[illegible]

FRONT USB PORT 0,1

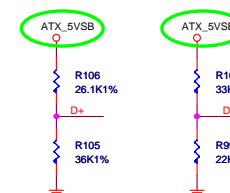
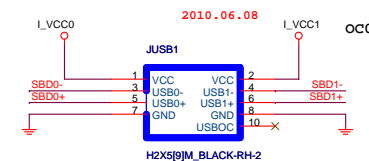


SIO GPIO pin 15

Default low

LOW= support I charge

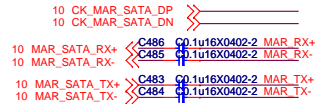
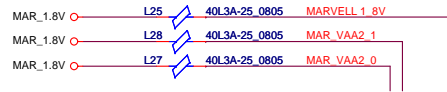
1st boot H/W default support i charge



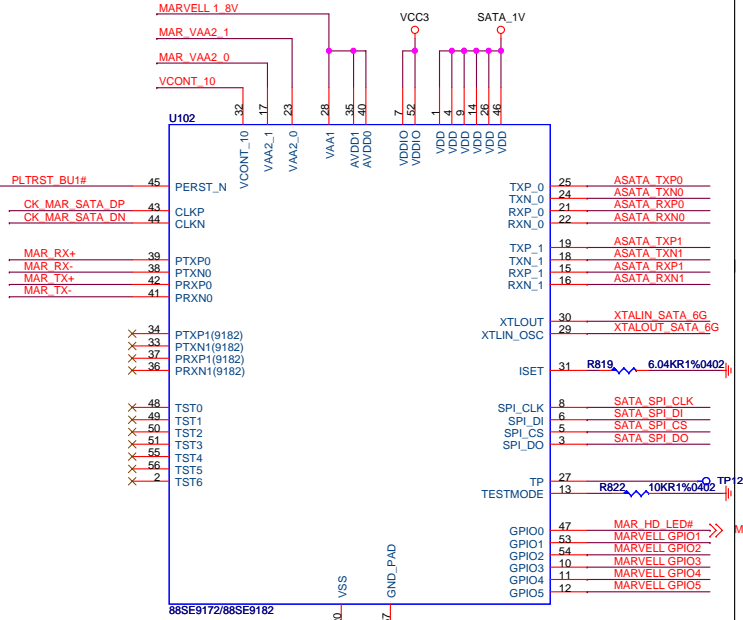
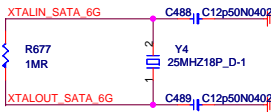
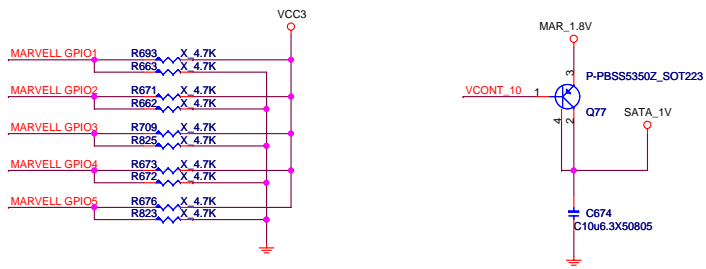
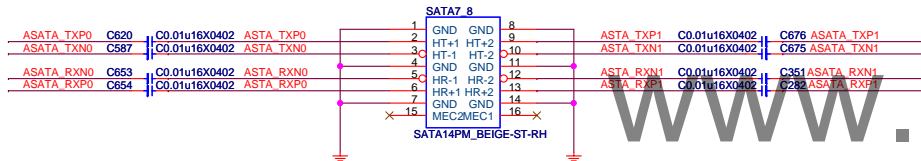
MICRO-STAR INT'L CO.,LTD

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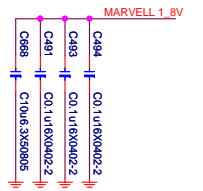
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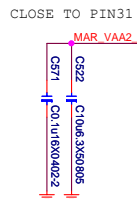
SATA 6G PORT 7,8



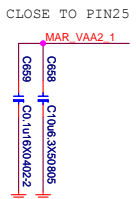
SATA_1.8V 100 mA



SATA_VAA2_0 70mA

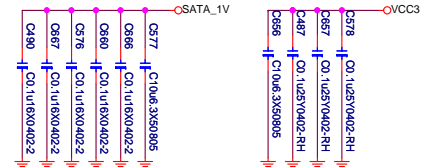


SATA_VAA2_1 70mA



SATA_1V 500 mA

CLOSE TO PIN5, 13, 21, 51, 64, 71



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